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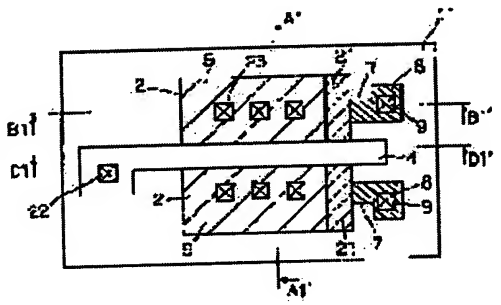
(54) FIELD-EFFECT TRANSISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To eliminate or suppress a reduction in an effective channel width, by a method wherein a region of low impurity concentration is provided in a source/drain region across a part of an extension region or a gate electrode.
SOLUTION: A source/drain region 5 is not provided in and on a semiconductor layer 2 in a partial region of the semiconductor layer 2, and a low impurity concentration band 21 where impurity is introduced at low concentration is formed. An extension region 7 projecting from the low impurity concentration band 21 to a channel widthwise direction is provided. A p+ region 8 where p type impurity is introduced into a part of the extension region 7 at high concentration is provided, and a body contact 9 is provided in a p region and is connected to a wire composed of aluminum. Holes generated in a channel part pass through a low concentration region below a source/drain region and the low impurity concentration band 21, and flow in the p+ region 8 formed in the extension region 7 and are excluded through the body contact 9. As a result, it is possible to eliminate or suppress a reduction in an effective channel width.



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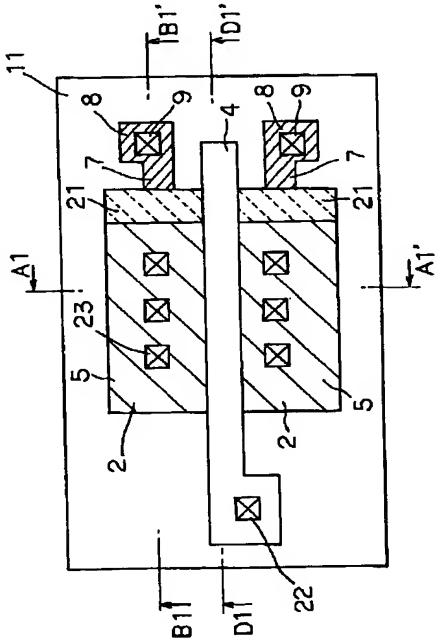
(54)【発明の名称】　電界効果型トランジスタ

(57)【要約】
【課題】　ＳＯＩＭＯＳＦＥＴにおいて、基板浮遊効果の原因となる正孔の排除。実効的なチャネル幅を減らさず、ソース・ドレインについて対称なボディコンタクト構造を提供。
【解決手段】　酸化膜上１の半導体層２上に、ゲート絶縁膜３を介してゲート電極４を設け、ゲート電極の両側のソースドレイン領域５の下部、またはその横の低不純物濃度帯２１に低濃度部を設け、さらに突起した延長領域７を設け、延長領域７中にｐ＋領域８を設ける。低不純物濃度帯２１に隣接するチャネル形成領域ではゲート酸化膜が厚く、不純物濃度が高い。



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【特許請求の範囲】

【請求項１】　酸化膜上の半導体層上に、ゲート絶縁膜を介してゲート電極を設け、ゲート電極の両側の半導体層において、少なくともその上部は第一導電型の不純物が高濃度に導入されたソース／ドレイン領域をなし、ソース／ドレイン領域の下部の領域またはゲート電極を挟んでソース／ドレイン領域に隣接する領域が不純物を低い濃度に導入した領域をなし、

該不純物濃度の低い領域から、ゲートとソース／ドレイン領域の境界に平行な方向に突起した、半導体よりなる延長領域が設けられ、

延長領域において少なくとも一部に第二導電型不純物を高濃度に導入した領域がチャネルに隣接せずに設けられ、

該第二導電型不純物を高濃度に導入した領域とソース／ドレイン領域の間には、延長領域の一部またはゲート電極を挟む該ソース／ドレイン領域に隣接する領域において、不純物濃度が低い領域が設けられていることを特徴とする電界効果型トランジスタ。

【請求項２】　前記ソース／ドレイン領域に接地電位が与えられる状態で、前記ソース／ドレイン領域の下部の全てが空乏層になることを特徴とする請求項１の電界効果型トランジスタ。

【請求項３】　チャネルが形成されるしきい値となる電圧が前記ゲート電極に加えられたときに、前記ゲート電極下部に位置する半導体層が、全てが空乏層になることを特徴とする請求項１の電界効果型トランジスタ。

【請求項４】　前記ゲート電極を挟んでかつ前記ソース／ドレイン領域に隣接する領域に不純物を低い濃度に導入した領域を持たず、ソース／ドレイン領域の下部の領域が不純物を低い濃度に導入した領域をなし、前記第二導電型不純物を高濃度に導入した領域と前記ソース／ドレイン領域の間には、前記延長領域の一部において、不純物濃度が低い領域を設けることを特徴とする請求項１の電界効果型トランジスタ。

【請求項５】　前記ソース／ドレイン領域の一部が半導体層の下部境界まで達する、請求項１の電界効果型トランジスタ。

【請求項６】　前記ソース／ドレイン領域の全てが半導体層の下部境界まで達し、前記ゲート電極を挟んで、ソース／ドレイン領域に隣接する領域に不純物を低い濃度に導入した領域を設けることを特徴とする、請求項１の電界効果型トランジスタ。

【請求項７】　前記延長領域の一部に設けられた第二導電型不純物を高濃度に導入した領域が、酸化膜の下にある半導体層または導電体層に接続されることを特徴とする、請求項１の電界効果型トランジスタ。

【請求項８】　前記延長領域に高不純物濃度の第二導電型領域を設けず、延長部に金属を直接接触させる、請求項１の電界効果型トランジスタ。

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【請求項９】　ゲート電極を挟んでソース／ドレインが形成されない半導体層に隣接し、ゲート電極下部に半導体層に位置する領域において、ゲート電極とその下に位置する半導体層の間に、他の領域のゲート絶縁膜よりも厚い絶縁膜を設けることを特徴とする、請求項１の電界効果型トランジスタ。

【請求項１０】　ゲート電極を挟んでソース／ドレインが形成されない半導体層に隣接し、ゲート電極下部に位置する半導体層において、ゲート電極下の他の領域よりも、第二導電型不純物の濃度を高くすることを特徴とする、請求項１の電界効果型トランジスタ。

【請求項１１】　前記延長領域の一部またはゲート電極を挟む前記ソース／ドレイン領域に隣接する領域において設けられる、不純物濃度が低い領域の上部の絶縁層上に、ソースに接続した配線が位置する、請求項１の電界効果型トランジスタ。

【請求項１２】　前記延長領域の一部またはゲート電極を挟む該ソース／ドレイン領域に隣接する領域において設けられる、不純物濃度が低い領域の上部の絶縁層上に、前記第二導電型不純物を高濃度に導入した領域に接続した配線が位置する、請求項１の電界効果型トランジスタ。

【請求項１３】　酸化膜上の半導体層上に形成される電界効果型トランジスタにおいて、第一導電型ソース／ドレイン領域をエピタキシャル層より形成し、その下に低濃度領域を持ち、低濃度領域がソース／ドレイン領域から離れた領域で第二導電型の高不純物濃度領域に接続される、請求項１の電界効果型トランジスタ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＬＳＩ等の半導体装置に用いられる電界効果型トランジスタに関し、特に絶縁体上に形成されるＳＯＩトランジスタに関するものである。

【０００２】

【従来の技術】絶縁体上の半導体層に形成される電界効果型トランジスタ、すなわちＳＯＩ－ＭＯＳＦＥＴにおいて起る基板浮遊効果と呼ばれる異常動作を抑制するために、いくつかの電界効果型トランジスタ構造が提案されている。基板浮遊効果とは、絶縁体上の半導体（ＳＯＩ；Silicon on insulator）層に正孔が蓄積することにより、ＳＯＩ層の電位が変動して異常動作が起きることをいい。これを防ぐためにはＳＯＩ層中の正孔を排除する方法を講じる必要がある。

【０００３】図２４、図２５に示すｎチャネル電界効果型トランジスタが大村によってアイイーイーイー、トランザクションズ、オブ、エレクトロンデバイシズ、３１巻、８号、１３９１ページ（IEEE Trans. Electron Devices, Vol.35, No.8, p.1391）に記されている。ここで図２４は平面図、図２５は断面図である。

【０００４】半導体層上にゲート絶縁膜を介してゲート電極１０２が設けられ、ゲート電極１０２を挟んでソース１０１、ドレイン１０３が設けられている。ドレイン領域１０３はｎ型不純物を高濃度に導入したｎ⁺領域よりなり、ソース領域１０１にはｎ型不純物を高濃度に導入したｎ⁺領域１０４と、ｐ型不純物を高濃度に導入したｐ⁺領域１０５が設けられている。半導体層（ＳＯＩ層１０８）は埋め込み酸化膜１０９上に形成されている。

【０００５】ゲート電極１０２下のチャネル形成領域において生成された正孔は、ゲート電極１０２の下に位置する半導体層を経由して、ｐ⁺領域１０５に隣接する領域まで流れ、その後ｐ型領域１０５を通して排除される。これは正孔がｎ⁺領域には流入できないが、ゲート下部の半導体層をチャネル幅方向（ゲートとソース／ドレイン領域の境界に平行な方向）に流れることは可能であること、およびｐ⁺領域には容易に流入できることをそれぞれ利用するものである。このトランジスタはこのように正孔を排除することにより、基板浮遊効果を抑制している。

【０００６】図２６に示すｎチャネル電界効果型トランジスタが、公開特許公報、平７－２２１３１４号に記されている。ｎ⁺領域からなるソース１０１、ドレイン１０３から離れた位置において、ゲート電極１０２に隣接する半導体層に、ｐ⁺領域１０５が設けられている。このトランジスタは、ゲート電極を軸にソース／ドレイン方向に対称であるという特徴をもつ。

【０００７】また、図３０のような構造が、ファーブレーグによって１９９２年アイイーディーエム、テクニカル、ダイジェスト、３３７頁に掲載されている。この構造ではソース領域１０２の上部がｎ⁺型領域（１０４）、下部がｐ型領域（１０５）によって構成され、アルミ配線１１１がｎ⁺型領域、ｐ型領域の双方に接触している。ソース領域上部のｎ⁺型領域は、通常のソースと同じく電子の供給源として作用する。ソース領域下部のｐ⁺領域１０５は図２４におけるｐ⁺領域１０５と同様に正孔を流入させ、これをチャネル形成領域から排除する作用をもつ。ｐ⁺型領域に流入した正孔は配線を通して排除されるか、あるいはｎ⁺領域へのトンネリングと電子との再結合により排除される。

【０００８】同様にソースの下にｐ⁺領域を設ける構造は公開特許公報、平２－１５９７６７号、平３－９４４７１号にも記載されている。

【０００９】図２４，２５，３０の構造ではｐ⁺領域はｎ⁺領域と配線によって互いに接続されている。また配線が設けられない場合においても、高濃度のｎ型層と高濃度のｐ型層の間では、バンド間トンネルにより導通するので、電気的に接続されることになる。

【００１０】また、図２７，２８のように、分離領域（素子領域でない領域）の半導体層を除去せず、その代わり分離領域の半導体層の上部にフィールドシールド電極（ＦＳゲート１２２）を設ける方法が、岩松らによって特開平７－９４７５４公報に記載されている。

【００１１】ここで図２７は平面図、図２８はＡ１０４－Ａ１０４'における断面図である。

【００１２】この場合、正孔はＦＳゲート１２２の下部を通り、ボディコンタクト１３３を通して排除される。

【００１３】また、図２９のような構造が、公開特許公報、平５－１１４７３４に記載されている。これは、ＳＯＩ層１０８上にｎ⁺ポリシリコン１４５よりなるソース／ドレイン領域を設けるとともに、ソース１０１からみてゲート電極１０２の反対側に、ｐ⁺領域１０５、ｐポリシリコン１４６を設ける。チャネル領域で発生した正孔はソース／ドレイン領域の下部を通り、ｐ⁺領域１０５、ｐ＋ポリシリコン１４６から排除される。

【００１４】

【発明が解決しようとする課題】ｎチャネルトランジスタを例に、従来技術の課題について述べる。

【００１５】図２４，２５，２６に示す従来技術による構造においては、ｐ⁺領域１０５がゲート電極１０２に接する領域において、有効にチャネルが形成されないという、第一の課題を持つ。ｎチャネルトランジスタにおいては、チャネルを形成する電荷はｎ⁺型のソースから供給されるが、ｐ⁺領域１０５が設けられると、この領域からはチャネルを形成する電荷が供給されず、ソースの実効的な幅が減少してしまう。これはチャネル幅（ソース／ドレインとゲートの境界の長さ）の実効値が低下することになる。チャネル幅の実効値が減ると、チャネルを流れる電流が減る。ｐ⁺領域を設けると、Ｐ領域に隣接するゲート電極の下部には、ゲート容量（ゲートとチャネル間の負荷容量）が付くので、その分だけゲート容量が増しているにもかかわらず、実効的なチャネル幅を増加させる寄与がないので、ｐ⁺領域を設けない場合に比べて、動作速度が低下する。

【００１６】この課題は、正孔をゲート下部においてチャネル幅方向（ソース／ドレイン領域とゲートの境界に平行な方向）に流してｐ⁺領域に導き、ｐ型領域から正孔を排除するという動作原理に起因して、必然的に発生するものである。

【００１７】また、図２４，２５，２９，３０の構造では、トランジスタの構造がゲート電極を軸に対称でないという第二の課題を持つ。

【００１８】一般の電界効果型トランジスタにおいては、ソース／ドレイン領域は同じ構造を持ち、互いに交替可能である。それに対して、これらの従来例は、ｐ⁺領域を持つ領域はソースとしてのみ用いられ、ドレインとすることができない。これは高電圧側となるドレインにｐ⁺領域があると、ｐ⁺領域は高電圧となるｎ⁺領域に接続されているために、それ自身も高電圧となるので、ドレイン側のＰ⁺領域とソース側のｎ領域が順バイ

アスとなり、ゲートにＯＦＦ信号が入力された状態においても、大量の漏れ電流が流れるためである。

【００１９】トランスファゲート、ＤＲＡＭ（ダイナミックランダムアクセスメモリ）セル等に用いられるトランジスタは、ソース／ドレイン領域のいずれが高電圧側となるかは、回路動作に依存して動的に変化する。これらの目的に用いるためには、トランジスタの構造が対称的であり、状況に応じて、ソース／ドレイン領域が交替可能でなければならない。したがって、非対称なトランジスタは、トランスファゲート、ＤＲＡＭセル等に用いることができない。

【００２０】また、ゲートアレイ等のＬＳＩでは、予め用途を決めずに拡散層等を形成しておき、後から、用途に応じて配線パターンを決める。したがって、ソース／ドレイン領域のいずれがソースとなり、ドレインとなるかが確定するのは、配線パターンが確定してからであり、拡散層形成時には確定していない。したがって、ゲートアレーにおいては、ソース／ドレイン領域が互換であるトランジスタを形成しておく必要があり、ソース、ドレインの役割が固定される非対称なトランジスタを用いることができない。

【００２１】また、非対称な構造を作成するには、p^+領域を、ゲート電極の上にかかるようにパターニングされたレジスト等をマスクにして、イオン注入によってソース／ドレイン領域の一方だけに作る必要があるが、ゲート長（ソースとドレインを結ぶ方向におけるゲート電極の幅）が短いトランジスタでは、このようなレジストのパターニング作業は極めて困難となる。

【００２２】また、ＳＯＩトランジスタは分離領域（ソース、ドレイン、チャネルがいずれも形成されない領域）に半導体層がないために、分離領域において、配線－半導体層、またはゲート－半導体層との間に寄生容量が付かない。しかし、図２７，２８の構造ではフィールドシールド電極（ＦＳゲート）を設けることにより、配線やゲートとフィールドシードル電極間に寄生容量が付くために、ＳＯＩトランジスタの長所が失われるという、第三の課題を持つ。また、この構造では、フィールドシールド電極を形成するために工程が複雑になるという第四の課題を持つ。

【００２３】図２９の構造では、ボディコンタクト（１０５、１４６）がソース１０１から見てゲート１０２の反対側にあるので、図３１に示すように、トランジスタが連続して接続されるようなパターンには用いることができないという、第五の課題を持つ。また、ソース／ドレイン領域をポリシリコンにより形成するが、ポリシリコンは通常、ソースやドレインが形成される単結晶シリコンに比べ、寄生抵抗が大きいという第六の課題を持つ。

【００２４】図２７，２８，２９の構造では、いずれもボディコンタクト用の配線パターンが必要となるという第七の課題を持つ。ＳＯＩ素子の特徴では、ウェルコンタクトを省略して、配線を単純化できるという特徴を持つが、これらの構造ではその長所が失われる。

【００２５】

【課題を解決するための手段】本発明は、上記従来技術の電界効果型トランジスタの有する課題の解決をその目的としてなされたものである。

【００２６】本発明の電界効果型トランジスタは、酸化膜上の半導体層上に、ゲート絶縁膜を介してゲート電極を設け、ゲート電極の両側の半導体層において、少なくともその上部は第一導電型の不純物が高濃度に導入されたソース／ドレイン領域をなし、ソース／ドレイン領域の下部の領域またはゲート電極を挟んでソース／ドレイン領域に隣接する領域（低不純物濃度帯）が不純物を低い濃度に導入した領域をなし、該不純物濃度の低い領域から、ゲートとソース／ドレイン領域の境界に平行な方向に突起した、半導体よりなる延長領域が設けられ、延長領域において少なくとも一部に第二導電型不純物を高濃度に導入した領域が設けられ、該第二導電型不純物を高濃度に導入した領域とソース／ドレイン領域の間には、延長領域の一部またはゲート電極を挟む該ソース／ドレイン領域に隣接する領域において、不純物濃度が低い領域が設けられていることを特徴としている。

【００２７】上記の構成によって、本発明においては、正孔はソース／ドレイン領域下部の低不純物濃度領域、またはその横の低不純物濃度領域を経て、延長部に達し、第二導電型不純物を高濃度に導入した領域から排除される。

【００２８】従来技術における前述の第一の課題は、正孔をゲート下部においてチャネル幅方向に流してチャネル形成領域（ゲート電極下部の半導体領域）に接して設けられたp^+型領域に導き、p^+型領域から正孔を排除するという構造に起因して、発生する。

【００２９】これに対して、本発明では、正孔を低不純物濃度領域においてチャネル幅方向に対して垂直な方向に流し、低不純物濃度領域に隣接するp^+領域から正孔を排除している。ソース／ドレイン領域下部の低不純物濃度領域、またはその横の低不純物濃度領域が正孔をチャネル幅方向に対して垂直な方向に流すための経路となるので、チャネル形成領域に接してp^+型領域を設ける必要がない。したがってp^+領域を設けることにより実効的なチャネル幅が減る問題を解消または抑制でき、第一の課題が解消または抑制される。

【００３０】特に、ゲート電極を挟みかつソース／ドレイン領域に隣接した領域に不純物が低い濃度に導入した領域（低不純物濃度帯）を持たず、該第二導電型不純物を高濃度に導入した領域とソース／ドレイン領域の間には、該延長領域の一部において、不純物濃度が低い領域を設けた場合、チャネル幅の実効的な減少は全くない。

【００３１】また、ゲート電極を挟みかつソース／ドレ

イン領域に隣接した領域に、不純物を低い濃度に導入した領域（低不純物濃度帯）を設ける場合においても、p⁺領域をゲート電極に隣接して設ける場合に比べて、その幅を狭くできるので、チャネル幅の実効的な減少を抑制できる。

【００３２】その理由は以下の通りである。p⁺領域をゲート電極に隣接して設ける場合、その中に配線と接続するコンタクト領域を設ける必要がある。したがって、従来技術におけるp⁺領域は、コンタクトの幅、および、それを囲む一定のマージンを含むだけの幅が必要となり、正孔の排除に最低限必要な幅よりも大きな幅が必要になる。本発明の構造においては、正孔を排除するためのコンタクトはゲートから離れた延長領域に取るので、この問題は生じず、該ソース／ドレイン領域に隣接した不純物を低い濃度に導入した領域の幅を小さくできる。

【００３３】また、第二導電型不純物を高濃度に導入した領域とソース／ドレイン領域の間には、不純物濃度の低い低不純物濃度帯、延長部があり、これらの領域に空乏層が形成されるので、p⁺領域とn領域との間の空乏層により電界が緩和され、バンド間トンネルによる導通が妨げられる。従ってp⁺領域がn領域の電位に連動することが妨げられる。

【００３４】したがって、第二導電型不純物を高濃度に導入した領域がドレイン側にあっても、p⁺領域の電位が上昇しないので漏れ電流は流れない。第二導電型不純物を高濃度に導入した領域をドレイン側に設けることができ、対称構造が得られるので、非対称構造に起因する、前述の第二の課題が、解決される。また、フィールドシールド電極を設けないので、第三、第四の課題が解決される。また、ボディコンタクトがソース／ドレイン領域から見て、チャネル幅方向にあるので、第五の課題が解決される。

【００３５】また、ソース／ドレイン領域に接地電位が与えられる状態で、ソース／ドレイン領域の下部の全てが空乏層になるように、ソース／ドレイン領域下部の第二導電型の不純物濃度を低く設定する。

【００３６】すると、ソース／ドレイン領域の下では空乏層がＳＯＩ層の下まで届く。これにより、ドレイン領域下部の寄生容量が低減するので、動作速度が向上する。また、正孔は電位の低いところを流れるが、空乏層の電位はソース／ドレイン領域よりも低いので、ソース領域下部の空乏層が正孔の経路とならしめることができる。

【００３７】また、チャネルが形成されるしきい値となる電圧がゲート電極に加えられたときに、ゲート電極下部に位置する半導体層が、全て空乏層となるように、半導体層の不純物濃度を設定する。ゲート電極下部に位置する半導体層が、全てが空乏層になると（完全空乏化すると）、正孔が蓄積しにくくなる。これは正孔の排除能力に関する負担を減らし、本発明の効果をより顕著ならしめることができる。

【００３８】本発明はゲート電極に接してp⁺領域を設けず、不純物濃度の低い領域を通して正孔をp⁺領域に導く。不純物濃度の低い領域はp⁺領域に比べて正孔を流す能力が劣るが、完全空乏化により正孔の蓄積を減らすことにより、正孔を流す能力が劣るという問題を相殺できる。

【００３９】また、ゲート電極を挟みかつソース／ドレイン領域に隣接した領域に、不純物を低い濃度に導入した領域を持たず、該第二導電型不純物を高濃度に導入した領域とソース／ドレイン領域の間には、該延長領域の一部において、不純物濃度が低い領域を設ける。

【００４０】この場合においても、ソース／ドレインの下を経由して正孔を排出できるので、前述の第二の課題を解決できる。

【００４１】また、延長領域の一部に設けられた第二導電型不純物が、酸化膜の下にある半導体層または導電体層に接続されることができる。トランジスタに接して配線に接したボディコンタクトを設ける必要がなく、前述の第七の課題を解決できる。

【００４２】また、ソース／ドレイン領域をエピタキシャル層より形成し、その下に低濃度領域を設け、低濃度領域がソース／ドレイン領域から離れた領域で第二導電型の高不純物濃度領域に接続されるようにすると、ソース／ドレインが単結晶になるので、前述の第六の課題が解決される。

【００４３】また、延長領域に高不純物濃度の第二導電型領域を設けず、延長部に金属を直接接触させる。

【００４４】また、ゲート電極を挟んでソース／ドレインが形成されない半導体層に隣接し、ゲート電極下部に半導体層に位置する領域において、ゲート電極とその下に位置する半導体層の間に、他の領域のゲート絶縁膜よりも厚い絶縁膜を設ける。あるいは、ゲート電極を挟んでソース／ドレインが形成されない半導体層に隣接し、ゲート電極下部に位置する半導体層において、ゲート電極下の他の領域よりも、第二導電型不純物の濃度を高くする。

【００４５】これらにより、ゲート電極を挟んでソース／ドレインが形成されない半導体層に隣接し、ゲート電極下部に半導体層に位置する領域のしきい値電圧を高くして、チャネルの形成を抑制できる。すると低不純物濃度帯２１にはチャネルが形成され難くなり、この部分にゲート－チャネル間の容量が付かなくなる。これにより、ゲート－チャネル間の容量が減らずにソース／ドレイン領域の有効幅が減るという前述の第一の課題に関連する問題が軽減される。

【００４６】また、該延長領域の一部またはゲート電極を挟む該ソース／ドレイン領域に隣接する領域において設けられる、不純物濃度が低い領域上の絶縁膜上に、ソ

ースに接続した配線が位置するようにする。

【００４７】あるいはこれらの領域の上部に、該第二導電型不純物を高濃度に導入した領域に接続した配線が位置するようにする。

【００４８】これらの領域がソースに接続した配線または該第二導電型不純物を高濃度に導入した領域に接続した配線に覆われると、これらの低不純物濃度領域は接地電位（または配線の電位）よりも低くなる。正孔は電位の低いところを流れるので、これらの領域に正孔が流れやすくなる。

【００４９】

【発明の実施の形態】以下、図面を参照しながら本発明の実施の形態について述べる。

【００５０】図１に本発明に基づく電界効果型トランジスタの平面図をｎチャネルトランジスタの場合について示す。図１のＡ１－Ａ１'断面、Ｂ１－Ｂ１'断面をそれぞれ図２、図３に示す。

【００５１】酸化膜１１上の半導体層２の上に、ゲート電極４が設けられる。ゲート電極４を挟む半導体層２において、その上部はｎ$^+$型ソースドレイン領域５をなし、半導体層２の下部は低い濃度の不純物を拡散したｐ$^-$領域２６をなす。ゲート電極４の下部にはゲート絶縁膜３が設けられ、ゲート電極の下部の半導体層２はチャネル形成領域２７をなす。ソース／ドレイン領域５上にはソース／ドレインコンタクト２３が設けられアルミニウム２４よりなる配線に接続される。但し、素子構造を解りやすくするために、アルミニウム２４は図３おいてのみ示す。

【００５２】半導体層２の一部領域では半導体層内、層上のいずれにもソース／ドレイン領域５が設けられず、不純物が低濃度に導入された低不純物濃度帯２１をなす。さらに低不純物濃度帯２１からチャネル幅方向に突起した、延長領域７が設けられる。ただし、ここでチャネル幅方向とはソース／ドレイン領域とゲート電極の境界に並行な方向をいう。延長領域７の少なくとも一部にはｐ型不純物を高濃度に導入したｐ$^+$領域８が設けられ、ｐ領域にはボディコンタクト９が設けられ、アルミニウム２４よりなる配線に接続される。ボディコンタクト９に接続される配線は、接地電位を保つか、あるいは少なくとも半導体層のバンドギャップよりも小さな電位、例えばシリコンであれば１．１２Ｖ以下の電位を保つ。ボディコンタクトに接続される配線の電位は、接地されるか、負である場合に、ボディコンタクトの正孔排除能力が高くなる。しかし、接地電位よりも電位が高くとも、ある程度の排除能力が得られる。しかしバンドギャップに相当する電位よりも高くなると、ボディコンタクトからソースへの漏れ電流が顕著になるので、これは避ける必要がある。

【００５３】この構造において、チャネル部において発生した正孔は、ソース／ドレイン領域下部の低濃度領域２６および低不純物濃度帯２１を経て、延長領域７に形成されたｐ$^+$領域８へと流れ込み、ボディコンタクト９を通して排除することができる。したがって、基板浮遊効果の原因となる正孔は排除されることになる。

【００５４】従来技術における第一の課題（実効的なチャネル幅の低下）は、正孔をゲート下部においてチャネル幅方向に流してｐ$^+$領域に導き、チャネル形成領域（ゲート電極下部の半導体領域）に接して設けたｐ$^+$型領域から正孔を排除するという構造に起因して、発生する。

【００５５】これに対して、本発明では、正孔を低不純物濃度領域（２１、２６）においてチャネル幅方向に対して垂直な方向に流し、低不純物濃度領域に隣接するｐ$^+$領域８から正孔を排除する。ソース／ドレイン領域下部の低不純物濃度領域２６、またはその横の低不純物濃度領域２１が正孔をチャネル幅方向に対して垂直な方向に流すための経路となるので、チャネル形成領域に接してｐ$^+$型領域を設ける必要がない。したがって、ｐ$^+$領域を設けることにより実効的なチャネル幅が低下するという問題を解消または抑制でき、前述の第一の課題が解決される。

【００５６】特に、低不純物濃度帯２１を持たず、ソース／ドレイン領域とｐ$^+$領域の間に低濃度領域３２が設けられ、ソース／ドレイン領域の下に低濃度領域２６を持つ構造（図１３、及びそのＢ１３－Ｂ１３'断面、図１４）では、チャネル幅の実効的な減少は全くない。また、低不純物濃度帯２１を設ける場合においても、ｐ$^+$領域をゲート電極に隣接して設ける場合に比べて、低不純物濃度帯２１の幅を狭くできるので、チャネル幅の実効的な減少を抑制できる。

【００５７】その理由は以下の通りである。従来例（図２４，２５，２６）のようにｐ$^+$領域１０５をゲート電極に隣接して設ける場合、その中に配線と接続するコンタクト領域を設ける必要がある。したがって、従来技術におけるｐ$^+$領域は、コンタクトの幅、および、それを囲む一定のマージンを含むだけの幅が必要となり、正孔の排除に最低限必要な幅よりも大きな幅が必要になる。本発明の構造においては、正孔を排除するためのコンタクトはゲートから離れた延長領域７にとるので、低不純物濃度帯２１の幅を小さくでき、前述の第一の課題を抑制できる。

【００５８】ｐ$^+$領域８とソース／ドレイン領域５は、低不純物濃度帯２１又はｐ領域３２によって隔離されているので、互いの導通はない。すなわち、両者（ｐ$^+$領域とソース／ドレイン）が隔離されることにより、両者間の電界強度が緩和される。従って、ドレインが高い電位になる場合においても、強電界が原因となって両者間にバンド間トンネル電流が流れることを防げる。よって、ｐ$^+$領域がドレイン側にあっても、ドレインとボディコンタクト間の漏れ電流は流れない。したがって、ボ

ディコンタクトをソース／ドレイン領域の両方に設けることができ、前述の第二の課題（非対称性）を解決することができる。

【００５９】また、図２４、２６の従来例のように、p⁺領域に接して、ゲートの下に位置する半導体層を正孔の経路として設ける必要がないので、ゲート電極とその半導体層との間の寄生容量が付かない。また、図２７の従来例のようなフィールドシールド電極を設けないので前述の第三、第四の課題を解決する事ができる。

【００６０】またソース／ドレイン領域からチャネル幅方向に延長した部分にボディコンタクトを設けるので、ゲートアレイ等トランジスタ連続して接続した構造にも適用することができる。よって、前述の第五の課題を解決される。

【００６１】以下、他の実施の形態について述べる。

【００６２】ソース／ドレイン領域に接地電位が与えられる状態で、第一導電型ソース／ドレイン領域の下部の全てが空乏層になるように、ソース／ドレイン領域下部の第二導電型の不純物濃度を低く設定することができる。

【００６３】すると、ソース／ドレイン領域の下では空乏層がＳＯＩ層の下まで届く。これにより、ドレイン領域下部の寄生容量が低減するので、動作速度が向上する。また、正孔は電位の低いところを流れるが、空乏層の電位はソース／ドレイン領域よりも低いので、ソース領域下部の空乏層が正孔の経路になることができる。

【００６４】また、チャネルが形成されるしきい値となる電圧がゲート電極に加えられたときに、ゲート電極下部に位置する半導体層が、全て空乏層となるように、半導体層の不純物濃度を設定することができる。ゲート電極下部に位置する半導体層が、全てが空乏層になると、その領域の電位が上がるので正孔が蓄積しにくくなる。これは正孔の排除能力に関する負担を減らし、本発明の効果をより顕著ならしめることができる。

【００６５】本発明はゲート電極に接してp⁺領域を設けず、不純物濃度の低い領域を通して正孔をp⁺領域に導く。不純物濃度の低い領域はp⁺領域に比べて正孔を流す能力が劣るが、完全空乏化により正孔の蓄積を減らすことにより、正孔を流す能力が劣るという問題を相殺できる。

【００６６】また、図４，５，６および７はp⁺領域８が配線２４に接続されず、ボディプラグ１５によってシリコン基板１０と接続される場合の本発明の実施の形態の説明図で、図４、図５はボディプラグ１５がp⁺領域を貫く場合、図６、図７はp⁺領域を貫かないでその側面から接する場合である。図８はボディプラグ１５がp⁺領域８に下から接する場合である。

【００６７】p⁺領域８はその直下のシリコン基１０板に接続され正孔はシリコン基板１０に排出されるので、p⁺領域と接地線を接続する配線を作る必要がない。またシリコン基板１０に、ボディプラグ１５と接する部分に埋め込みp⁺領域２８を設ける場合を図９、図１０に示す。シリコン基板１０に埋め込みp⁺領域を設けると、シリコン基板内の正孔の導通が改善される。

【００６８】図１の構造においてソース／ドレイン領域をエピタキシャル層３０により形成する場合を図１１に示す。エピタキシャル層からのリンを浅く拡散させることにより、半導体層の表面にn⁺領域３１が浅く形成される。

【００６９】図１において、低不純物濃度帯２１を設けない場合を図１３、図１４に示す。この場合は延長領域７のうち、ソース／ドレイン領域に接する部分に、p⁻領域３２を設ける。この場合、延長領域７中のp⁻領域３２が、低不純物濃度帯２１に代わって、p⁺領域とソース／ドレイン領域５との間の電界を緩和する作用を持つ。また低不純物濃度帯２１と延長領域７中のp⁻領域３２の両方を設けても良い。

【００７０】また、低不純物濃度帯２１を設ける場合で、ソース／ドレイン領域５が半導体層２の裏側に達する場合のＢ１－Ｂ１'における断面図を図１５に示す。この場合は正孔はゲート電極下のチャネル領域をチャネル幅方向に流れ、低不純物濃度帯２１に達した後、延長領域７から排出される。この場合、ソース／ドレイン領域がＳＯＩ層の下に達してもよいので、ソース／ドレイン領域の形成に対して、浅い接合を形成する必要がない。

【００７１】また、図１３の構造において、延長部にp⁺領域を設けず、金属を直接接触させ、ショットキーコンタクト（配線２４と低濃度層２１の接続部）を取る場合を図１７に示す。この場合、配線にタングステン、タングステンシリサイド等を用いても良い。また、ショットキー障壁の大きさを調整するために、低濃度層２１と配線２４の間に中間層として、ＴｉＮ、タングステンシリサイド等の金属、あるいは金属元素を含む化合物を挟んでも良い。この場合、ショットキーコンタクトは、低濃度層２１と中間層とによって形成される。

【００７２】低濃度の半導体層に金属を接触させたショットキーコンタクトは、整流性を持つ。ショットキーコンタクトを形成する金属を接地する場合（金属側の電位が低い場合）のバンド図を図３２に示す。余剰な正孔は金属側へ流れることができるが、電子はチャネル側からも、金属側からも、低濃度の半導体層（p⁻領域）に形成される障壁のために流れることができない。また、金属側の電位が高い場合を図３３、図３４に示す。もしp型不純物濃度の高いp基板に金属を接触させると、図３３のようになり、金属に接触するp基板において空乏層が形成される領域に、薄い障壁が形成され、正孔はこの障壁をトンネル現象により通り抜けるので、金属側から余計な正孔電流が注入されることになる。これに対して、本発明のように金属が低濃度のp⁻領域、または真

性（ｉ）領域に接触する場合を図３４に示す。この場合、低濃度領域、ｉ領域はドレイン電圧の影響を受け、ドレイン電位に近い電圧になるので、図３４のように正孔に対する障壁が形成され、正孔が注入されない。これは特に図１３のように、低濃度領域がドレイン下の低濃度領域を介してのみチャネルに接続する場合に図３４に示すように、ドレイン電界の影響を受けた領域が障壁となるので、効果が顕著になる。

【００７３】また、図１８はゲートアレイ等、トランジスタが複数個連結されて配置される場合、図１の構造を連結した状態を示し、図１９はp^+領域８を延長し、ボディコンタクト９をゲート電極に対するコンタクト２２よりも外側に設けた例を示す。図１８のように、ボディコンタクトは、p^+領域を覆うように開けられてよい。（コンタクトを囲むようなp^+領域のマージンを取らない）。

【００７４】また、ゲートアレイにおいて、ソースとなる電極においては、ボディコンタクトとソースを互いに接続する。ドレインとなる領域においては、p^+領域上部にコンタクトホールを開けないようにする。これにより、ドレインとなる領域においては、p^+領域上部をドレインに接続する配線が通過する場合も、通過しない場合のいずれにおいても、p^+領域とドレイン電極が電気的に短絡することを防ぐことができる。

【００７５】トランスファゲートのように、ソース／ドレイン領域のいずれが高電圧側になるかが確定しない場合には、ボディコンタクトをソース／ドレイン領域と接続せず、ボディコンタクトは全て接地する。すなわち接地電位を持つ配線に接続する。

【００７６】また、図２０に、ソース／ドレイン領域下部の低濃度領域がn^-型である場合を示す。

【００７７】p^-シリコン基板を接地すると、仕事関数の関係から、p^-基板はソースよりも低い電位となる。また、シリコン基板に負の電位を与えても、同様にシリコン基板はソースよりも低い電位となる。すると、ソース／ドレイン領域の下にn^-領域を設けても、基板からの電界の影響によりこの領域には空乏層が形成される。空乏層が形成されると、n^-領域４０の電位が下がるので、正孔とは極性の異なるｎ型であるにも係らず、正孔が流れやすくなる。

【００７８】図２１は低不純物濃度帯２１に挟まれた領域（低不純物濃度帯に隣接するチャネル領域）上の酸化膜をゲート酸化膜より厚くした場合を示す（図２１の中間絶縁膜４１、図２１は図１のＤ１－Ｄ１’断面に相当）。中間絶縁膜４１を設けると、この部分のしきい値電圧が上がる。これはゲート酸化膜が厚いとしきい値電圧が上がるという原理による。すると低不純物濃度帯２１に隣接する領域にはチャネルが形成され難くなり、この部分にゲートチャネル間の容量（ゲート容量）が付かなくなる。

【００７９】これにより、低不純物濃度帯２１を設けることにより、ソース／ドレイン領域の有効幅が減ることの影響を低減できる。ゲートーチャネル間の容量が減らずに、ソース／ドレイン領域の有効幅が減ると、動作速度に対して不利であるが、ソース／ドレイン領域の有効幅とともに、ゲートーチャネル間の容量が減れば動作速度に対するデメリットを低減できる。

【００８０】また、中間絶縁膜４１は低不純物濃度帯２１上を覆っても良い。この場合、低不純物濃度帯とその上に配置される配線間の容量分を軽減できるという効果が得られる。

【００８１】また、低不純物濃度帯のｐ型不純物濃度帯を増しておくと、この部分のしきい値電圧が上がり、チャネルが形成されなくなるので、この方法によってもソース／ドレイン領域が有効に働かない部分（低不純物濃度帯２１に挟まれた部分）において容量が付くという問題を軽減できる。

【００８２】また、低不純物濃度帯２１、または延長部の低不純物濃度領域３２を、ボディコンタクトに接続する配線４２で覆うことができる。低不純物濃度帯２１、または延長部の低不純物濃度領域３２にｐ型不純物を導入すると、これらの領域はその上部にある配線よりも電位が低くなる。ボディコンタクトが接地電位にあると、これらの低不純物濃度領域（２１、３２）は接地電位よりも低くなる。正孔は電位の低いところを流れるので、これらの領域（２１、３２）に正孔が流れやすくなる。

【００８３】また、図１３の構造において低不純物濃度帯２１、または延長部の低不純物濃度領域３２を、ソース／ドレイン領域に接続する配線４３で覆った例を図２３に示す。ソース／ドレイン領域の一方はソースとして動作するが、ソース側は電位が低いので、その結果上述の接地線で覆った場合と同様に、ソース側で低不純物濃度領域に正孔が流れやすくなり、正孔が排除されやすくなる。

【００８４】

【実施例】

実施例１

図１に本実施例に基づく電界効果型トランジスタの平面図を示す。図１のＡ１－Ａ１’断面、Ｂ１－Ｂ１’断面をそれぞれ図２、図３に示す。

【００８５】酸化膜１１上の半導体層２の上に、半導体層２を横断するようにn^+ポリシリコンよりなる幅０．２５ミクロンのゲート電極４が設けられる。ゲート電極４の下部には厚さ５ｎｍのゲート絶縁膜３が設けられる。ゲート電極４を挟む半導体層２において、その上部は高濃度にｎ型の不純物を拡散したソースドレイン領域５をなし、半導体層２の下部は低い濃度にｐ型の不純物を拡散したp^-領域２６をなす。ゲート電極の下部の半導体層２はチャネルが形成される、チャネル形成領域２７をなす。ソース／ドレイン領域５上にはソース／ドレ

インコンタクト２３が設けられアルミニウム２４よりなる配線に接続される。

【００８６】半導体層２の一部はソース／ドレイン領域５が設けられず、p^- 型の低不純物濃度帯２１をなす。さらに低不純物濃度帯２１からチャネル幅方向に突起した、延長領域７が設けられる。ただし、ここでチャネル幅方向とはソース／ドレイン領域とゲート電極の境界に並行な方向をいう。延長領域７の少なくとも一部にはｐ型不純物を高濃度に導入したp^+ 領域８が設けられ、p^+ 領域にはボディコンタクト９が設けられ、アルミニウム２４よりなる配線に接続される。ボディコンタクト９に接続される配線は、接地電位を保つか、あるいは少なくとも半導体層のバンドギャップよりも小さな電位、例えばシリコンであれば１．１２Ｖ以下の電位を保つ。

【００８７】図２、図３の断面図において、１０はシリコン基板、１１は埋め込み酸化膜、２５は層間絶縁膜を示す。埋め込み酸化膜、層間絶縁膜の厚さはそれぞれ４００ｎｍとした。ＳＯＩ層の厚さは６０ｎｍ、ソース／ドレイン領域５の厚さは２０ｎｍ、低不純物濃度帯２１のチャネル幅方向に対する幅は１ミクロン、ソース／ドレイン領域のチャネル幅方向に対する幅は１０ミクロンとした。延長領域のＡ１－Ａ１’方向に並行な方向の幅は０．３ミクロンとした。p^- 領域２６にはホウ素が$1\times10^{17}cm^{-3}$、低不純物濃度帯２１にはホウ素が$1\times10^{17}cm^{-3}$、p^+ 領域８にはホウ素が$1\times10^{19}cm^{-3}$、ソース／ドレイン領域にはリンが$1\times10^{19}cm^{-3}$導入された。シリコン基板は濃度$1\times10^{16}cm^{-3}$のホウ素を含んだp^- 型とした。

【００８８】この構造において、チャネル部において発生した正孔は、ソース／ドレイン領域下部の低濃度領域２６および低不純物濃度帯２１を経て、延長領域７に形成されたp^+ 領域８へと流れ込み、ボディコンタクト９を通して排除することができる。したがって、基板浮遊効果の原因となる正孔は排除されることになる。

【００８９】p^+ 領域８とソース／ドレイン領域５は、低不純物濃度帯２１によって隔離されているので、互いの導通はない。すなわち、ソースだけでなく、ドレイン領域においても、p^+ 領域との間にバンド間トンネル等によって漏れ電流が流れることがない。したがって、ボディコンタクトをソース／ドレイン領域の両方に対称的に設けることができる。また、ボディコンタクトの形成に伴う、実効チャネル幅の減少がない。またソース／ドレイン領域がチャネル幅方向に延長した部分にボディコンタクトを設けるので、ゲートアレイ等トランジスタが連続して接続した構造にも適用することができる。

【００９０】実施例２

本実施例は、図１において、p^+ 領域８が配線に接続されず、シリコン基板１０と接続されている場合である。

【００９１】図４、図６は本実施例の、それぞれp^+ 領域８付近を拡大した平面図、図５、図７はそれぞれ図４、図６におけるＣ４－Ｃ４’、Ｃ６－Ｃ６’断面における立面図である。いずれにおいてもp^+ 領域８はp^+ ポリシリコンよりなるボディプラグ１５によってp^- シリコン基板１０と接続されている。図４、図５はp^+ 領域を貫く場合、図６、図７はp^+ 領域を貫かないでその側面から接する場合である。図８はボディプラグがp^+ 領域の下から接する場合である。p^+ 領域はその直下のシリコン基板に接続され、正孔はシリコン基板へ流出するので、p^+ 領域と接地線を接続する配線を作る必要がない。

【００９２】またシリコン基板１０には、図９、図１０に示すように、ボディプラグ１５と接する部分に埋め込みp^+ 領域２８を設けてもよい。p^+ 領域２８はトランジスタから離れた位置において、埋め込み酸化膜を貫く第二のp^+ ポリシリコンプラグ２９、およびアルミニウム２４よりなる配線によって接地線と接続される（図９）。また、プラグの材料としてアルミニウム２４のような金属を用いてもよい（図１０）。シリコン基板１０に埋め込みp^+ 領域を設けると、シリコン基板内の正孔の導通をよくすることができた。ボディプラグ１５は、プラグ材料（p^+ポリシリコン、金属、金属シリサイド等の導電体）のＣＶＤ等による埋め込みと、続くＲＩＥ等によるエッチバックを行うことにより形成される。

【００９３】実施例３

本実施例は、図１の構造において、ソース／ドレイン領域をエピタキシャル層３０により形成した場合で、図１のＡ１－Ａ１’断面について本実施例の断面図を図１１に示す。エピタキシャル層３０には高濃度のリンが導入された。ランプアニールや電気炉による熱処理により、エピタキシャル層からのリンを浅く拡散させることにより、半導体層の表面にn^+ 領域３１が浅く形成された。n^+ 領域３１の厚さは例えば２０ｎｍである。

【００９４】実施例４

本実施例は、図１において、低不純物濃度帯２１を設けない場合で、図１３は平面図、図１３のＢ１３－Ｂ１３’断面を図１４に示す。この構造においては、延長領域７のうち、ソース／ドレイン領域に接する部分に、ホウ素を低濃度$1\times10^{17}cm^{-3}$に導入したp^- 領域３２を設けた。この場合、延長領域７中のp^-領域３２が、低不純物濃度帯２１に代わって、p^+ 領域とソース／ドレイン領域５との間の電界を緩和する作用を持つ。また低不純物濃度帯２１と延長領域７中のp^- 領域３２の両方を設けてもよい。

【００９５】実施例５

低不純物濃度帯２１を設ける場合は、ソース／ドレイン領域５が半導体層２の裏側に達してもよい。本実施例は、この場合の例で、その場合の断面図を（図１のＢ１－Ｂ１’断面に相当する位置において）図１５に示す。この場合は正孔はゲート電極下のチャネル領域を通り、低不純物濃度帯２１に達した後、延長領域７から排出さ

れる。この場合、ソース／ドレイン領域がＳＯＩ層の下に達してもよいので、ソース／ドレイン領域の形成に対して、浅い接合を形成する必要がなく、通常のイオン注入等、既存のプロセスを使えるというメリットがある（図１５）。

【００９６】実施例６

本実施例は図１３の構造において、延長部にp⁺領域を設けず、金属を直接接触させ、ショットキーコンタクトを取った場合で、図１３におけるＢ１３－Ｂ１３'断面を図１７に示す。また、ショットキーコンタクトがソース／ドレイン領域上のコンタクトと接続される場合を、同様な断面で図１６に示す。

【００９７】低濃度の半導体層に金属を接触させたショットキーコンタクトは、整流性を持つ。ショットキーコンタクトを形成する金属を接地する場合（金属側の電位が低い場合）のバンド図を図３２に示す。余剰な正孔は金属側へ流れることができるが、電子はチャネル側からも、金属側からも、低濃度の半導体層（p⁻領域）に形成される障壁のために流れることができない。また、金属側の電位が高い場合を図３３、図３４に示す。もしｐ型不純物濃度の高いｐ基板に金属を接触させると、図３３のようになり、金属に接触するｐ基板において空乏層が形成される領域に、薄い障壁が形成され、正孔はこの障壁をトンネル現象により通り抜けるので、金属側から余計な正孔電流が注入されることになる。これに対して、本発明のように金属が低濃度のp⁻領域、または真性（ｉ）領域に接触する場合を図３４に示す。この場合、低濃度領域、ｉ領域はドレイン電圧の影響を受け、ドレイン電位に近い電圧になるので、図３４のように正孔に対する障壁が形成され、正孔が注入されない。これは特に図１３のように、低濃度領域がドレイン下の低濃度領域を介してのみチャネルに接続する場合に図３４に示すように、ドレイン電界の影響を受けた領域が障壁となるので、効果が顕著になる。

【００９８】また、これにより図１６のようにソース／ドレイン領域とボディコンタクトを接続することが可能となる。すなわち、ソース／ドレイン領域が電位の低いソースとして作用する場合に、正孔がこれを通して排除されるとともに、電位の高いドレインとして作用する場合にもリーク電流が発生せず、対称な構造が可能になる。

【００９９】また、配線にタングステン、タングステンシリサイド等を用いても良い。また、ショットキー障壁の大きさを調整するために低濃度層２１と配線２４の間に中間層として、ＴｉＮ、タングステンシリサイド等の金属、あるいは金属元素を含む化合物を挟んでも良い。

【０１００】実施例７

本実施例は、ゲートアレイ等、トランジスタが複数個連結されて配置される場合、図１の構造を連結した例（図１８；平面図）と、p⁺領域８を延長し、ボディコンタクトがゲート電極に対するコンタクトよりも外側に設けられる場合の例（図１９；平面図）である。ボディコンタクトはp⁺領域を覆うように開けられ（コンタクトを囲むようなp⁺領域のマージンを取らない）ても良い（図１８）、ゲートアレイにおいて、ソースとなる電極においては、ボディコンタクトとソースを互いに接続する。ドレインとなる領域においては、p⁺領域上部にコンタクトホールを開けないようにする。これにより、ドレインとなる領域においては、p⁺領域上部をドレインに接続する配線が通過する場合も、通過しない場合のいずれにおいても、p⁺領域とドレイン電極が電気的に短絡することを防ぐことができる。

【０１０１】トランスファゲートのように、ソース／ドレイン領域のいずれが高電圧側になるかが確定しない場合には、ボディコンタクトをソース／ドレイン領域と接続せず、ボディコンタクトは全て接地する、すなわち接地電位を持つ配線に接続する。

【０１０２】実施例８

本実施例は、ソース／ドレイン領域下部の低濃度領域がn⁻型の場合で、その断面を（図１のＢ１－Ｂ１'断面に相当する位置において）図２０に示す。ソース／ドレイン領域の下部はリンを$1\times10^{17}cm^{-3}$注入したn⁻領域４０とした。シリコン基板１０はp⁻型とした。シリコン基板１０には接地電位（０Ｖ）または負の電位とした。

【０１０３】p⁻シリコン基板を接地すると、仕事関数の関係から、p⁻基板はソースよりも低い電位となる。また、p⁻シリコン基板に負の電位を与えた場合もp⁻よりも低い電位となる。すると、ソース／ドレイン領域の下にn⁻領域を設けても、シリコン基板の電位の影響を受け、この領域には空乏層が形成される。空乏層が形成されると、n⁻領域の電位が下がるので、正孔とは極性の異なるｎ型であるにも係らず、正孔が流れやすくなる。

【０１０４】実施例９

本実施例は、低不純物濃度帯２１に隣接するチャネル形成領域上の酸化膜をゲート酸化膜より厚くした場合の例である。

【０１０５】図１において、低不純物濃度帯２１とそれに隣接するチャネル形成領域（ゲート電極の下の領域）上に中間絶縁膜４１を設けた場合の、Ｄ１－Ｄ１'断面を図２１に示す。

【０１０６】中間絶縁膜４１を設けると、この部分のしきい値電圧が上がる。これはゲート酸化膜が厚いとしきい値電圧が上がるという原理による。すると低不純物濃度帯２１にはチャネルが形成され難くなり、この部分にゲート－チャネル間の容量が付かなくなる。

【０１０７】これにより、低不純物濃度帯２１を設けることにより、ソース／ドレイン領域の有効幅が減ることの影響を低減できる。ゲート－チャネル間の容量が減ら

ずに、ソース／ドレイン領域の有効幅が減ると、動作速度に対して不利であるが、ソース／ドレイン領域の有効幅とともに、ゲート－チャネル間の容量が減れば動作速度に対するデメリットを低減できる。

【０１０８】また、低不純物濃度帯のｐ型不純物濃度を増しておくと、この部分のしきい値電圧が上がり、チャネルが形成されなくなるので、この方法によってもソース／ドレイン領域が有効に働かない部分に対するゲート容量を軽減できる。

【０１０９】実施例１０

本実施例においては、図１の構造において低不純物濃度帯２１、または延長部の低不純物濃度領域３２を、ボディコンタクトに接続する配線４２で覆った例を図２２（平面図）に示す。

【０１１０】低不純物濃度帯２１、または延長部の低不純物濃度領域３２にｐ型不純物を導入すると、これらの領域はその上部にある配線よりも電位が低くなる。ボディコンタクトが接地電位にあると、これらの低不純物濃度領域は接地電位よりも低くなる。正孔は電位の低いところを流れるので、これらの領域に正孔が流れやすくなる。

【０１１１】また、図１３の構造において低不純物濃度帯２１、または延長部の低不純物濃度領域３２を、ソース／ドレイン領域に接続する配線４３で覆った例を図２３（平面図）に示す。

【０１１２】ソース／ドレイン領域の一方はソースとして動作するが、ソース側は電位が低いので、その結果上の場合と同様に、ソース側で低不純物濃度領域（２１、３２）に正孔が流れやすくなり、正孔が排除されやすくなる。

【０１１３】以上、ｎチャネルトランジスタについての実施例を示したが、ｐチャネルトランジスタの場合は、以上の実施例において、極性をすべて逆にすれば良い。

【０１１４】

【発明の効果】本発明の電界型トランジスタの構造において、チャネル部において発生した正孔は、ソース／ドレイン領域下部の低濃度領域２６および低不純物濃度帯２１を経て、延長領域２７に形成されたｐ$^+$領域８へと流れ込み、ボディコンタクト９を通して排除することができる。したがって、基板浮遊効果の原因となる正孔は排除される。

【０１１５】ｐ$^+$領域８とソース／ドレイン領域５は、低不純物濃度帯２１または延長部の低不純物濃度領域３２によって隔離されているので、互いの導通はない。すなわち、ソースだけでなく、ドレイン領域においても、ｐ$^+$領域との間にバンド間トンネル等によって漏れ電流が流れることがない。したがって、ボディコンタクトを両側のソース／ドレイン領域に対称的に設けることができる。

【０１１６】また、ゲートの下に正孔の経路となる半導体層を設ける必要がないので、ゲート電極とその半導体層との間の寄生容量が付かない。またソース／ドレイン領域をチャネル幅方向に延長した部分にボディコンタクトを設けるので、ゲートアレイ等トランジスタが連続して接続した構造にも適用することができる。

【０１１７】またボディプラグによりｐ$^+$領域とその直下のシリコン基板を接続すると、ｐ$^+$領域と接地線を接続する配線を作る必要がない。さらにｐ$^+$領域と接続されるシリコン基板１０に埋め込みｐ$^+$領域を設けると、シリコン基板内の正孔の導通をよくすることができる。

【０１１８】また、ソース／ドレイン領域の下に正孔を流す構造では、低不純物濃度帯２１を設けず、延長領域７のうち、ソース／ドレイン領域に接する部分に、不純物を低濃度に導入した領域を設ける。すると、延長領域中の低濃度領域が、ｐ$^+$領域とソース／ドレイン領域５との間の電界を緩和する作用を持つ。電界が緩和されれば、バンド間のトンネル電流が減り、漏れ電流が抑制される。

【０１１９】また、チャネル幅方向の一部の領域に低不純物濃度帯２１を設ける場合は、ソース／ドレイン領域５が半導体層２の裏側に達してもよい。この場合は正孔はゲート電極下のチャネル領域から、低不純物濃度帯２１に達した後、延長領域７から排出される。この場合、ソース／ドレイン領域がＳＯＩ層の下に達してもよいので、ソース／ドレイン領域の形成に対して、浅い接合を形成する必要がなく、通常のイオン注入等、既存のプロセスを使えるというメリットがある。

【０１２０】また、延長部７にｐ$^+$領域を設けず、金属を直接接触させ、ショットキーコンタクトを取ると、金属部が高電位となっても、その整流性により、余剰な電荷が金属部から流入することを防ぐとともに、ＳＯＩ層中の余剰な正孔を排除することができる。

【０１２１】また、ソースとなる電極においては、ボディコンタクトとソースを互いに接続する。ドレインとなる領域においては、ｐ$^+$領域上部にコンタクトホールを開けないようにする。これにより、配線を簡単にできるとともに、ドレインとなる領域においては、ｐ$^+$領域上部をドレインに接続する配線が通過する場合も、通過しない場合のいずれにおいても、ｐ$^+$領域とドレイン電極が電気的に短絡することを防ぐことができる。

【０１２２】ｎチャネル電界効果型トランジスタにおいて、ソース／ドレイン領域の下部に低濃度のｎ型領域を設け、埋め込み酸化膜下のシリコン基板を接地電位（０Ｖ）または負の電位とすると、ソース／ドレイン領域下のｎ$^-$領域に空乏層が形成され、正孔とは極性の異なるｎ型であるにも係らず、正孔が流れやすくなる。

【０１２３】第一導電型電界効果型トランジスタにおいて、ソース／ドレイン領域に隣接せず、かつゲート電極の下部に半導体層が位置する領域において、半導体層とゲート電極の中間に、中間絶縁膜２１を設ける。あるい

は、この領域の半導体層の第二導電型不純物の濃度を上昇させる。すると、この部分の半導体層におけるしきい値電圧が上がるので、この部分にゲート－チャネル間の容量が付かなくなる。これによりソース／ドレイン領域の有効幅が減ることによる動作速度におけるデメリットを低減できる。

【０１２４】ソース／ドレイン領域とｐ⁺領域の中間に位置する不純物濃度が低い領域（低不純物濃度帯２１、または延長部の低不純物濃度領域３２）を、ボディコンタクトに接続する配線またはソースに接続する配線で覆う。すると、これらの領域に正孔が流れやすくなり、ＳＯＩ層から正孔の排除が容易になる。

【図面の簡単な説明】

【図１】本発明の実施例を示す模式平面図
【図２】図１のＡ１－Ａ１’断面図
【図３】図１のＢ１－Ｂ１’断面図
【図４】本発明の別の実施例の模式平面部分図
【図５】図４のＣ４－Ｃ４’断面図
【図６】本発明の別の実施例の模式平面部分図
【図７】図６のＣ６－Ｃ６’断面図
【図８】本発明の別の実施例の模式断面部分図
【図９】本発明の別の実施例の模式断面図
【図１０】本発明の別の実施例の模式断面図
【図１１】本発明の別の実施例の模式断面図
【図１２】本発明の別の実施例の模式断面図
【図１３】本発明の別の実施例の模式平面図
【図１４】図１３のＢ１３－Ｂ１３’断面図
【図１５】本発明の別の実施例の模式断面図
【図１６】本発明の別の実施例の模式断面図
【図１７】本発明の別の実施例の模式断面図
【図１８】本発明のトランジスタが複数個連結されている実施例の模式平面図
【図１９】本発明のトランジスタが複数個連結されている別の実施例の模式平面図
【図２０】本発明の別の実施例の模式断面図
【図２１】本発明の別の実施例の模式断面図
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【図２３】本発明の別の実施例の模式平面図
【図２４】従来技術を示す模式平面図
【図２５】従来技術を示す模式断面図
【図２６】従来技術を示す模式平面図
【図２７】従来技術を示す模式平面図
【図２８】従来技術を示す模式断面図
【図２９】従来技術を示す模式断面図
【図３０】従来技術を示す模式断面図
【図３１】従来技術の問題点を説明する模式平面図
【図３２】本発明の効果を説明するバンド図
【図３３】従来技術の問題点を説明するバンド図
【図３４】本発明の効果を説明するバンド図

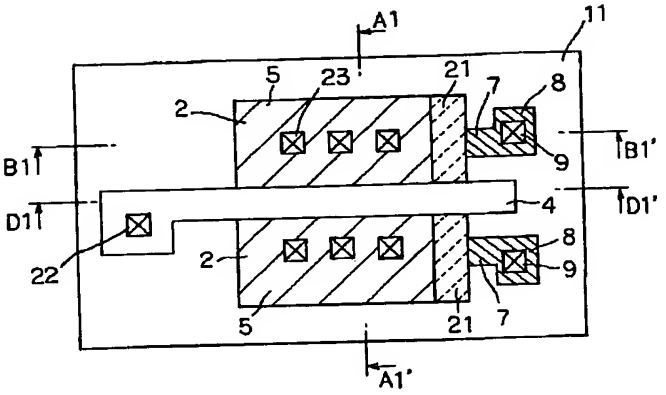
【符号の説明】

１　酸化膜
２　半導体層
３　ゲート絶縁膜
４　ゲート電極
５　ソースドレイン領域
７　延長領域
８　ｐ⁺領域
９　ボディコンタクト
１０　シリコン基板
１１　埋め込み酸化膜
１５　ボディプラグ
２１　低不純物濃度帯
２３　ソース／ドレインコンタクト
２４　アルミニウム
２５　層間絶縁膜
２６　ｐ⁻領域
２７　チャンネル形成領域
２８　埋め込みｐ⁺領域
２９　第二のｐ⁺ポリシリコンプラグ
３０　エピタキシャル層
３１　ｎ⁺領域
３２　ｐ⁻領域
４１　中間絶縁膜
４２　ボディコンタクトに接続する配線
４３　ソース／ドレイン領域に接続する配線
１０１　ソース
１０２　ゲート
１０３　ドレイン
１０４　ｎ⁺領域
１０５　ｐ⁺領域
１０６　ゲート酸化膜
１０７　ｐ領域
１０８　ＳＯＩ層またはｐ⁻領域
１０９　埋め込み酸化層
１１０　シリコン基板
１１１　アルミニウム配線
１１２　酸化膜
１２０　ｐ⁺領域
１２１　ｐ領域
１２２　ＦＳゲート
１２３　ＦＳゲート酸化膜
１２４　ゲート酸化膜
１２５　ゲート電極
１２６　第一の酸化膜
１２７　第二の酸化膜
１３０　ソース／ドレイン領域
１３１　ゲートコンタクト
１３２　ＦＳゲートコンタクト
１３３　ボディコンタクト
１３４　ｐ⁺⁺領域

１４１　ドレイン電極
１４２　ソース電極
１４３　配線電極

＊１４４　コンタクト
　１４５　n⁺ ポリシリコン
＊　１４６　p⁺ ポリシリコン

【図１】



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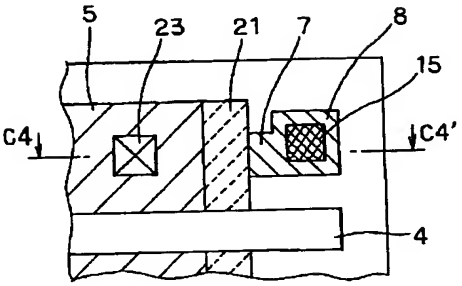

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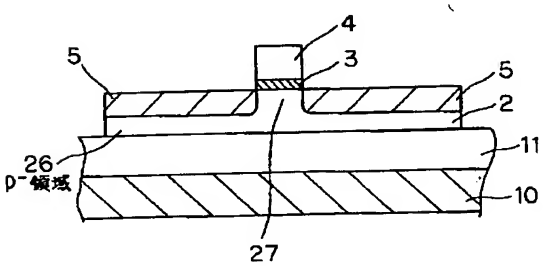

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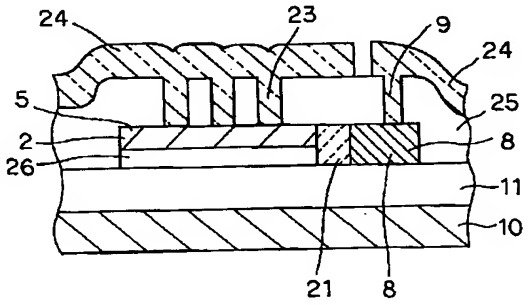

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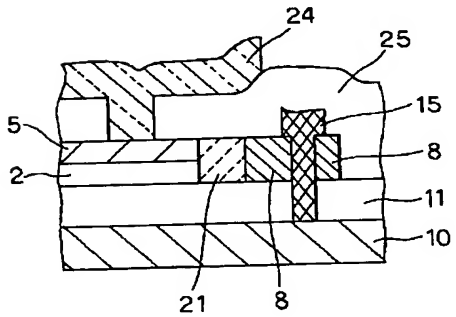

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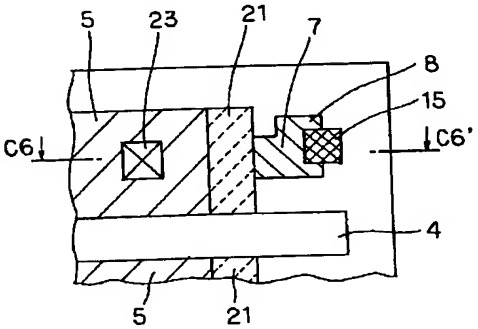

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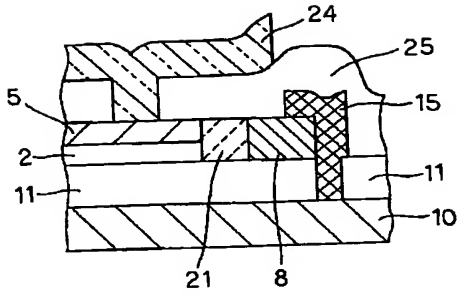

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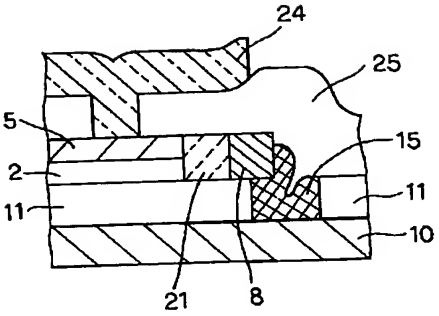

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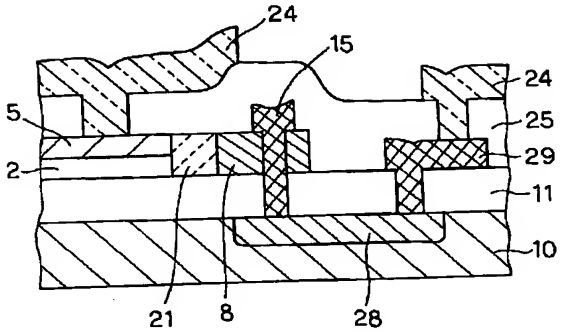

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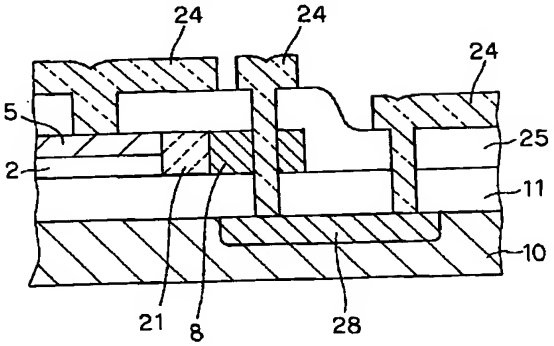

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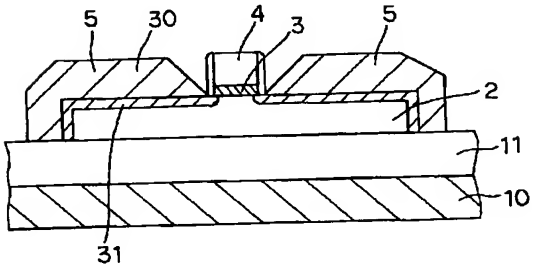

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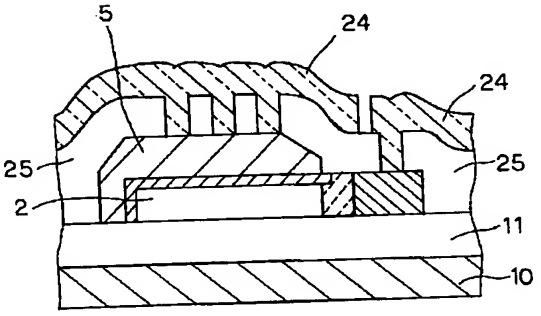

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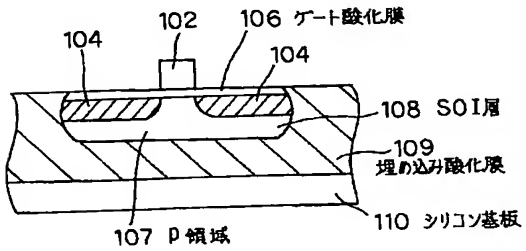

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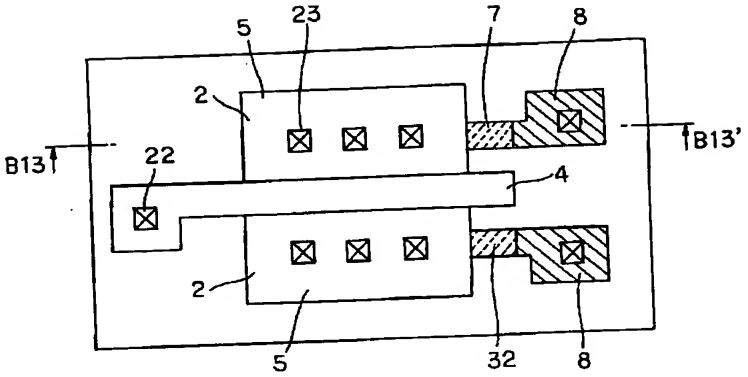

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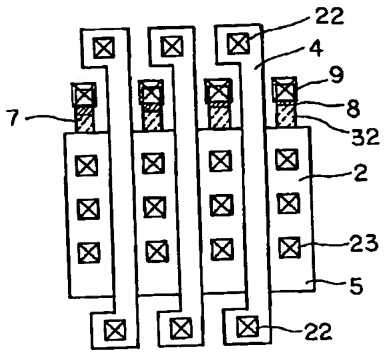

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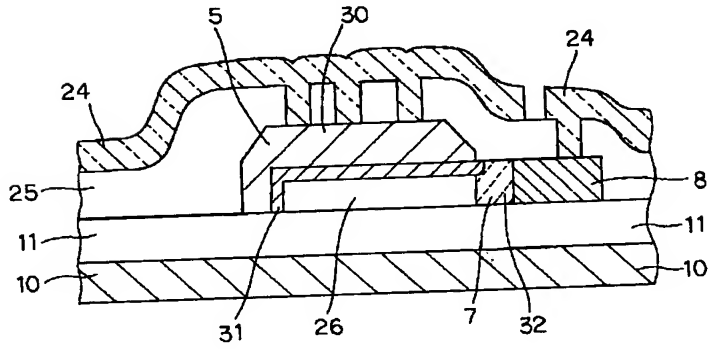

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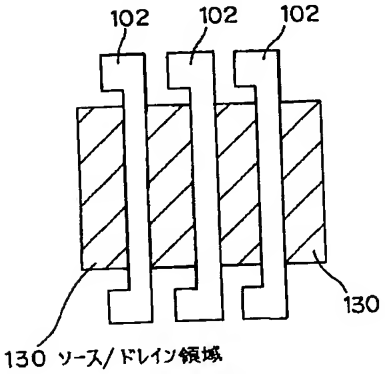

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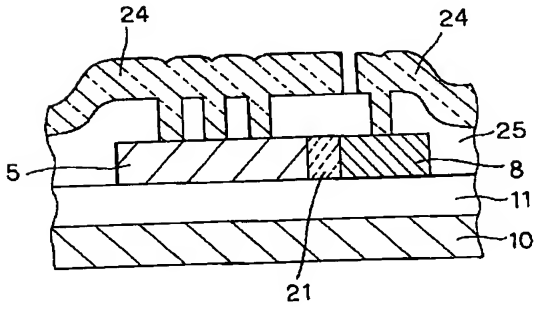

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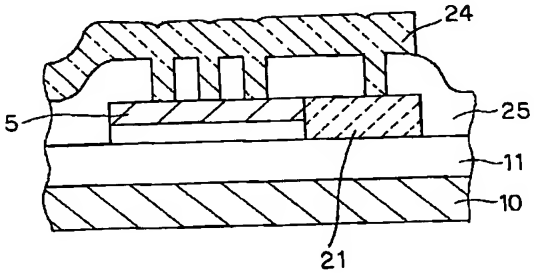

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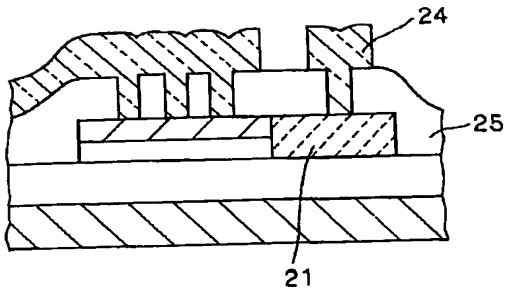

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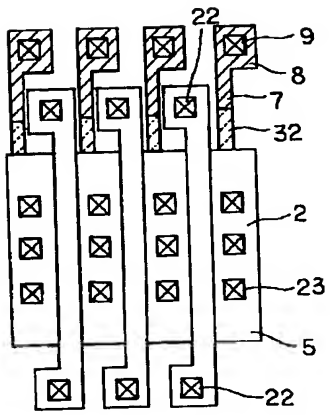

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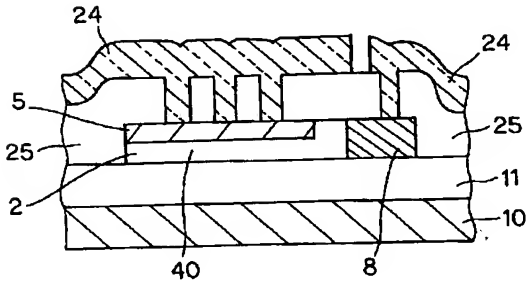

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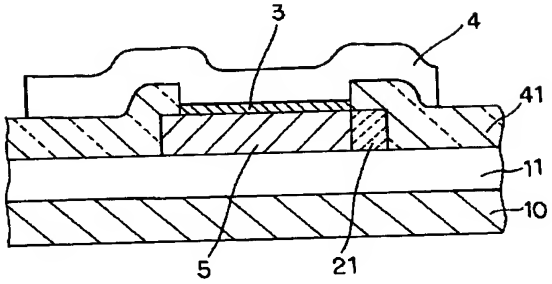

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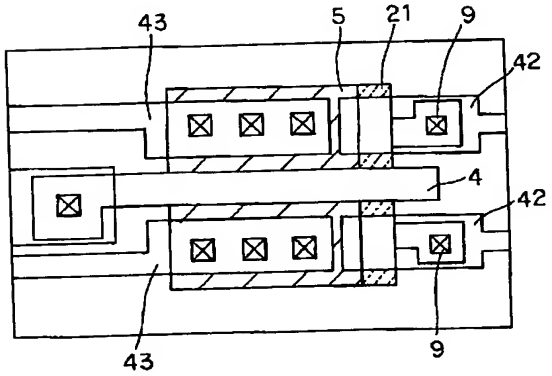

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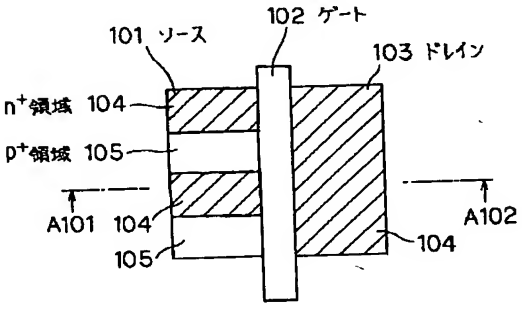

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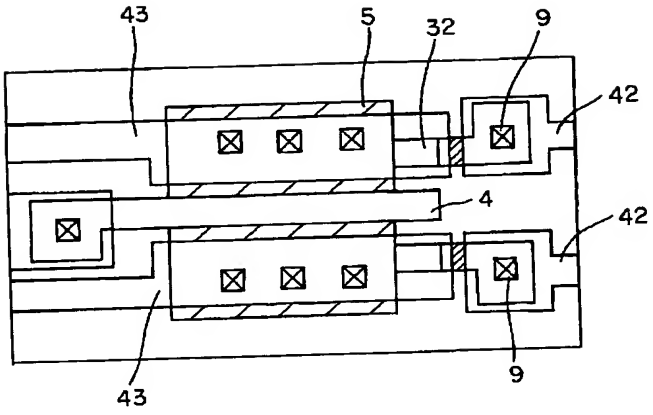

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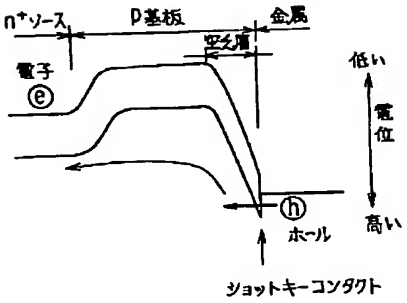

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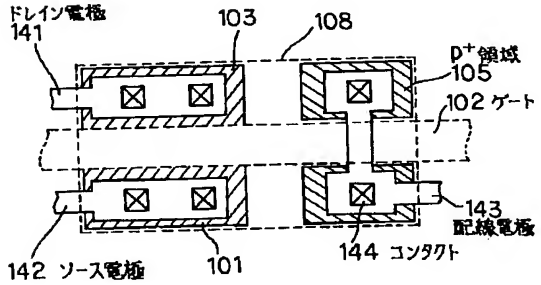

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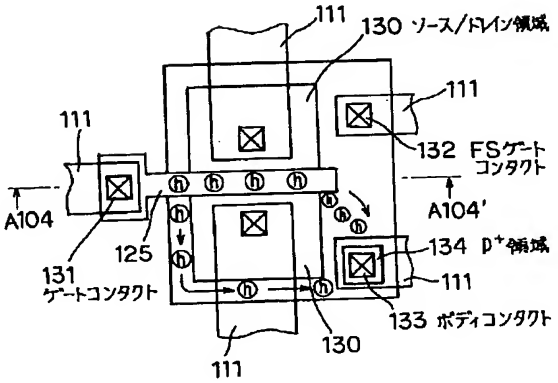

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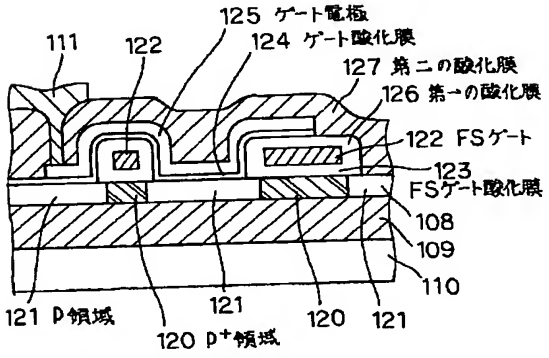

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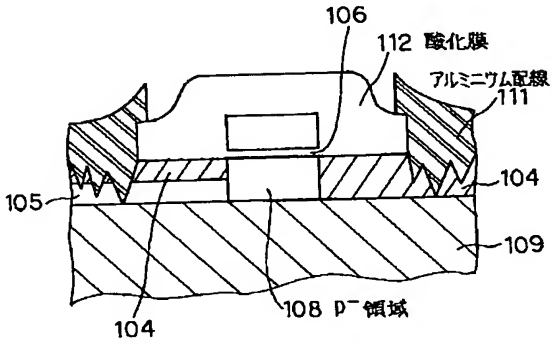

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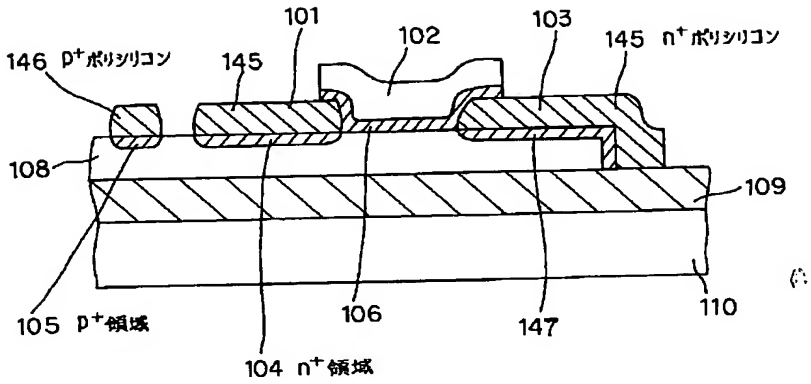
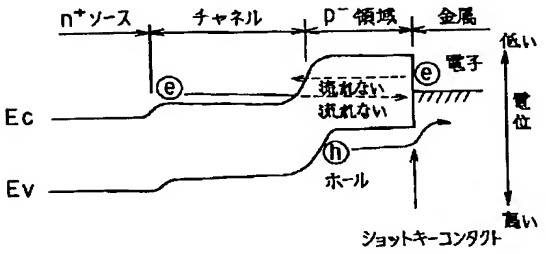
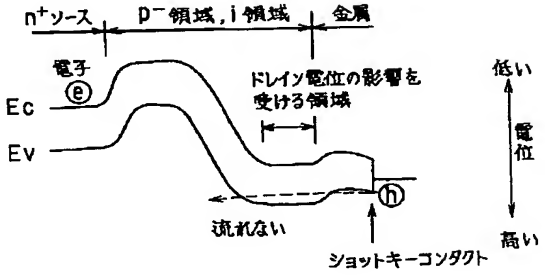

101
102
103
145 n+ポリシリコン
146 p+ポリシリコン
145
108
109
105 p+領域
106
147
110
104 n+領域

【図３２】


n+ソース
チャネル
p−領域
金属
低い
電位
高い
e
電子
流れない
流れない
Ec
Ev
h
ホール
ショットキーコンタクト

【図３４】


n+ソース
p−領域，i領域
金属
電子
e
ドレイン電位の影響を
受ける領域
低い
電位
高い
Ec
Ev
h
流れない
ショットキーコンタクト

PATENT ABSTRACTS OF JAPAN

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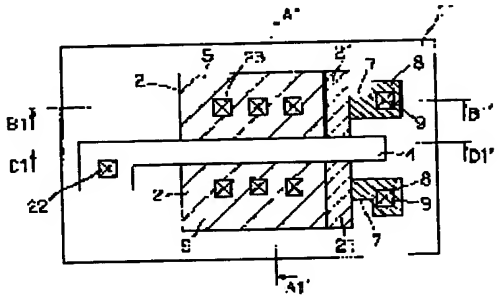
H01L 21/336

(21)Application number : 09-297473
(22)Date of filing : 29.10.1997

(71)Applicant : NEC CORP
(72)Inventor : KOU RISHIYOU

(54) FIELD-EFFECT TRANSISTOR

(57)Abstract:
PROBLEM TO BE SOLVED: To eliminate or suppress a reduction in an effective channel width, by a method wherein a region of low impurity concentration is provided in a source/drain region across a part of an extension region or a gate electrode.
SOLUTION: A source/drain region 5 is not provided in and on a semiconductor layer 2 in a partial region of the semiconductor layer 2, and a low impurity concentration band 21 where impurity is introduced at low concentration is formed. An extension region 7 projecting from the low impurity concentration band 21 to a channel widthwise direction is provided. A p+ region 8 where p type impurity is introduced into a part of the extension region 7 at high concentration is provided, and a body contact 9 is provided in a p region and is connected to a wire composed of aluminum. Holes generated in a channel part pass through a low concentration region below a source/drain region and the low impurity concentration band 21, and flow in the p+ region 8 formed in the extension region 7 and are excluded through the body contact 9. As a result, it is possible to eliminate or suppress a reduction in an effective channel width.



LEGAL STATUS

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[Date of sending the examiner's decision of rejection]	21.03.2001
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3216591
[Date of registration]	03.08.2001
[Number of appeal against examiner's decision of rejection]	2001-06178
[Date of requesting appeal against examiner's decision of rejection]	19.04.2001
[Date of extinction of right]	

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] On the semiconductor layer on an oxide film, prepare a gate electrode through a gate insulator layer, and it sets in the semiconductor layer of the both sides of a gate electrode. The upper part at least the source / drain field where the impurity of the first conductivity type was introduced into high concentration Nothing, The field where the field which adjoins the source / drain field on both sides of the lower field or lower gate electrode of the source / drain field introduced the impurity into low concentration Nothing, Projected from the low field of this high impurity concentration in the direction parallel to the boundary of the gate, and the source / drain field. The extended field which consists of a semiconductor is prepared and the field which introduced the second conductivity-type impurity into high concentration in part at least in the extended field is prepared, without adjoining a channel. The field effect transistor characterized by preparing the field where high impurity concentration is low in the field contiguous to this source / drain field whose part or gate electrode of an extended field is pinched between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field.
[Claim 2] The field effect transistor of the claim 1 to which all the lower parts of the aforementioned source / drain field are characterized by the bird clapper at a depletion layer in the state where grounding potential is given to the aforementioned source / drain field.
[Claim 3] The field effect transistor of the claim 1 to which all are characterized by the bird clapper by the semiconductor layer located in the aforementioned gate electrode lower part at a depletion layer when the voltage used as the threshold in which a channel is formed is applied to the aforementioned gate electrode.
[Claim 4] The field effect transistor of the claim 1 characterized by for high impurity concentration to prepare a low field in a part of the aforementioned extended field between the field which introduced nothing and the aforementioned second conductivity-type impurity into high concentration for the field where it did not have the field which introduced the impurity into low concentration in the field which adjoins aforementioned source / drain field on both sides of the aforementioned gate electrode, but the field of the lower part of the source / drain field introduced the impurity into low concentration, and the aforementioned aforementioned source / drain field.
[Claim 5] The field effect transistor of a claim 1 which a part of aforementioned source / drain field attain to the lower boundary of a semiconductor layer.
[Claim 6] The field effect transistor of a claim 1 which all aforementioned sources / drain fields reach to the lower boundary of a semiconductor layer, and whose aforementioned gate electrode is pinched, and is characterized by establishing the field which introduced the impurity into low concentration in the field contiguous to the source / drain field.
[Claim 7] The field effect transistor of a claim 1 characterized by connecting to the semiconductor layer or conductor layer under an oxide film the field which introduced into high concentration the second conductivity-type impurity prepared in a part of aforementioned extended field.
[Claim 8] The field effect transistor of a claim 1 which the second conductivity-type field of high high impurity concentration is not established [field effect transistor] in the aforementioned extended field, but contacts a metal to an extension directly.
[Claim 9] The field effect transistor of a claim 1 which adjoins the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode, and is characterized by preparing an insulator layer thicker than the gate insulator layer of other fields between a gate electrode and the semiconductor layer located in the bottom of it in the field located in the gate electrode lower part at a semiconductor layer.
[Claim 10] The field effect transistor of a claim 1 which adjoins the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode, and is characterized by making concentration of the second conductivity-type impurity higher than other fields under a gate electrode in the semiconductor layer located in the gate electrode lower part.
[Claim 11] The field effect transistor of a claim 1 to which wiring linked to the source is located on the insulating layer of the upper part of the fi ld which is prepared in the field contiguous to the aforementioned source / drain field whose part or gate electrod of the aforementioned extended fi ld is pinched, and where high impurity concentration is low.
[Claim 12] The field effect transistor of a claim 1 to which the wiring to which the aforementioned second conductivity-type impurity was connected to the field introduced into high concentration is located on the insulating layer of the upper part of the field which is prepared in the field contiguous to this source / drain field whose part or

gate electrode of the aforementioned extended field is pinched, and where high impurity concentration is low.
[Claim 13] The field effect transistor of a claim 1 which forms the first conductivity-type source / drain field from an epitaxial layer, and has a low concentration field in the bottom of it in the field effect transistor formed on the semiconductor layer on an oxide film and by which a low concentration field is connected to th high high-impurity-concentration field of the second conductivity type in the field distant from the source / drain field.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the SOI transistor formed especially on an insulator about the field effect transistor used for semiconductor devices, such as LSI.
[0002]
[Description of the Prior Art] In order to suppress unusual operation called field effect transistor formed in the semiconductor layer on an insulator, i.e., the substrate suspension effect which happens in SOI-MOSFET, some field-effect-transistor structures are proposed. The substrate suspension effect is good in changing the potential of a SOI layer and unusual operation occurring, when an electron hole is accumulated in the semiconductor (SOI;Silicon on insulator) layer on an insulator. In order to prevent this, it is necessary to devise the method of eliminating the electron hole in a SOI layer.
[0003] The n channel electric field effect type transistor shown in drawing 24 and drawing 25 is IEEE, transactions, OBU, electron DEBAISHIZU, 31 volumes, No. 8, and 1391 pages (IEEE Trans.Electron Devices, Vol.35, No.8, p.1391) by Omura. It is describing. Drawing 24 is a plan and drawing 25 is a cross section here.
[0004] The gate electrode 102 is formed through a gate insulator layer on a semiconductor layer, and the source 101 and the drain 103 are formed on both sides of the gate electrode 102. The drain field 103 is n+ which introduced n type impurity into high concentration. n+ which consisted of a field and introduced n type impurity into the source field 101 at high concentration A field 104 and p+ which introduced p type impurity into high concentration The field 105 is formed. The semiconductor layer (SOI layer 108) is formed on the embedding oxide film 109.
[0005] The electron hole generated in the channel formation field under the gate electrode 102 goes via the semiconductor layer located under the gate electrode 102, and is p+. It flows to the field contiguous to a field 105, and is eliminated through p type field 105 after that. For this, an electron hole is n+. It is [a possible thing and] p+ to flow the semiconductor layer of the gate lower part in the direction of channel width (direction parallel to the bour.dary of the gate, and the source / drain field), although it cannot flow into a field. It uses, respectively that it can flow into a field easily. By eliminating an electron hole in this way, this transistor has suppressed the substrate suspension effect.
[0006] The n channel electric field effect type transistor shown in drawing 26 is describing a open patent official report and common [No. 221314 / seven to]. n+ It is p+ to the semiconductor layer which adjoins the gate electrode 102 in the source 101 which consists of a field, and the position distant from the drain 103. The field 105 is formed. This transistor has the feature of being symmetrical with the source/the direction of a drain, centering on a gate electrode.
[0007] Moreover, structure like drawing 30 is carried on an AII dee em, technical one, a digest, and 337 pages by fur PUREGU in 1992. At this structure, the upper part of the source field 102 is n+. A type field (104) and the lower part are constituted by p type field (105), and the aluminum wiring 111 is n+. It is in contact with the both sides of a type field and p type field. n+ of the source field upper part A type field acts as an electronic source of supply as well as the usual source. p+ of the source field lower part A field 105 is p+ in drawing 24 . An electron hole as well as a field 105 is made to flow, and it has the operation which eliminates this from a channel formation field. p+ It is eliminated through wiring or the electron hole which flowed into the type field is n+. It is eliminated by the reunion of the tunneling to a field, and an electron.
[0008] It is p+ under the source similarly. The structure of preparing a field is indicated by a open patent official report, common [No. 159767 / two to], and common / No. 94471 / three to].
[0009] At drawing 24 and 25 or 30 structures, it is p+. A field is n+. It connects mutually with a field and wiring. Moreover, when wiring is not formed, since it flows with the tunnel between bands, between high-concentration n type layer and high-concentration p type layer, it will connect electrically.
[0010] Moreover, like drawing 27 and 28, the semiconductor layer of an isolation region (field which is not an element field) is not r moved, but th method of instead preparing a field screening electrode (FS gate 122) in the upper part of the semiconductor layer of an isolation region is indicated by Iwamatsu and oth rs at th JP,7-94754,A official report.
[0011] It is a cross section [in / A104-A104' / drawing 27 and / in drawing 28] here. / a plan
[0012] In this case, an electron hole passes along the lower part of the FS gate 122, and is eliminated through the body contact 133.
[0013] Moreov r, structure like drawing 29 is indicated by a open patent official report and common [5-114734].

This is n+ on the SOI layer 108. While preparing the source / drain field which consists of contest 145 polysilicon, it is p+ to the opposite side of the gate electrode 102, in view of the source 101. A field 105 and contest 146 p polysilicon ar formed. The electron hole generated in the channel field passes along the lower part of the source / drain field, and is p+. It is eliminated from a field 105 and contest 146 p+ polysilicon.
[0014]
[Problem(s) to be Solved by the Invention] An n channel transistor is stated to an example about the technical problem of the conventional technology.
[0015] It sets in the structure by drawing 24 and the conventional technology shown in 25 and 26, and is p+. A field 105 has the first technical problem [say / that a channel is not formed effectively] in the field which touches the gate electrode 102. The charge which forms a channel in an n channel transistor is n+. It is p+ although supplied from the source of type. If a field 105 is formed, from this field, the charge which forms a channel will not be supplied but the efficiency-width of face of the source will decrease. As for this, the actual value of channel width (the length of the boundary of the source/drain, and the gate) will fall. If the actual value of channel width decreases, the current which flows a channel will decrease. p+ Since a gate capacitance (load-carrying capacity between the gate and a channel) is attached to the lower part of the gate electrode which adjoins P field when a fi ld is prepared, although the gate capacitance of the part is increasing, since there is no contribution to which efficiency-channel width is made to increase, it is p+. A working speed falls compared with the case where a field is not prepared.
[0016] This technical problem passes an electron hole in the gate lower part in the direction of channel width (direction parallel to the boundary of the source / drain field, and the gate), and is p+. It leads to a field, it originates in the principle of operation of eliminating an electron hole from p type field, and generates inevitably.
[0017] Moreover, with drawing 24 and the structure of 25, 29, and 30, the structure of a transistor has the second technical problem are not symmetrical, centering on a gate electrode.
[0018] In a general electric field effect type transistor, the source / drain field can have the same structure, and can change it mutually. These conventional examples are p+ to it. The field with a field is used only as the source and cannot be used as a drain. This is p+ to the drain which becomes a high-voltage side. It is p+ when there is a field. A fi ld is n+ used as the high voltage. Since it connects with the field and becomes a high voltage also in itself, it is P+ by the side of a drain. Also in the state where the field and n field by the side of the source became forward bias, and the OFF signal was inputted into the gate, it is for a lot of leakage current to flow.
[0019] As for the transistor used for the transfer gate, a DRAM (dynamic RAM) cell, etc., any shall become a high-voltage side between the source / drain field changes dynamically depending on circuit operation. In order to use for these purposes, the structure of a transistor is symmetrical and the source / drain field must be able to be changed according to a situation. Therefore, an unsymmetrical transistor cannot be used for the transfer gate, a DRAM cell, etc.
[0020] Moreover, by LSI, such as a gate array, the diffusion layer etc. is formed without deciding a use beforehand, and a circuit pattern is decided afterwards according to a use. Therefore, it is decided any any of the source / drain field serve as the source, and serve as a drain after a circuit pattern is decided, and it is not decided at the time of diffusion layer formation. Therefore, it is necessary to form the transistor whose source / drain field are compatibility, and the source and the unsymmetrical transistor to which the role of a drain is fixed cannot be used in a gate array.
[0021] Moreover, it is p+ in order to create unsymmetrical structure. Although it is necessary to use as a mask the resist by which patterning was carried out so that a field may be started on a gate electrode, and it is necessary to make to either the source or a drain field with an ion implantation, with a transistor with short gate length (width of face of the gate electrode in the direction which connects a drain to the source), the patterning work of such a resist becomes very difficult.
[0022] Moreover, since a SOI transistor does not have a semiconductor layer in an isolation region (field in which no sources, drains, and channels are formed), in an isolation region, a parasitic capacitance is not attached between a wiring-semiconductor layer or a gate-semiconductor layer. However, with drawing 27 and the structure of 28, since a parasitic capacitance is attached to wiring, the gate, and field SHIDORU inter-electrode by preparing a field screening electrode (FS gate), it has the third technical problem [say / that the advantage of a SOI transistor is lost]. Moreover, with this structure, in order to form a field screening electrode, it has the fourth technical problem that a process becomes complicated.
[0023] With the structure of drawing 29 , since body contact (105 146) sees from the source 101 and is in the opposite side of the gate 102, as shown in drawing 31 , it has the fifth technical problem [say / that it cannot use] in a pattern to which a transistor is connected continuously. Moreover, although the source / drain field is formed with contest polysilicon, contest polysilicon usually has the sixth technical problem that parasitism resistance is strong, compared with the single crystal silicon with which the source and a drain are formed.
[0024] With drawing 27 and 28 or 29 structures, it has the seventh technical problem that the circuit pattern for body contact is all needed. Although it has the featur that well contact is omitted and wiring can be simplified, in th featur of a silicon-on-insulator desubstrate, the advantag is lost with such structur s.
[0025]
[Means for Solving the Problem] this invention is solved considering the t chnical probl m which the field effect transistor of the above-mentioned conventional technology has as the purpos .
[0026] The field effect transistor of this invention prepar s a gate electrode through a gate insulator layer on the

semiconductor layer on an oxide film, and sets it in the semiconductor lay r of the both sides of a gate electrode. The upper part at least the source / drain field where the impurity of the first conductivity typ was introduced into high concentration Nothing, The fi ld where the field (low high-impurity-concentration band) which adjoins th source / drain field on both sides of the lower field or lower gate electrode of the sourc / drain field introduced the impurity into low concentration Nothing, Projected from the low field of this high impurity concentration in the direction parallel to the boundary of the gate, and the source / drain field. The extended fi ld which consists of a semiconductor is prepared and the field which introduced the second conductivity-type impurity into high concentration in part at least in the extended field is prepared. It is characterized by preparing the field wh r high impurity concentration is low in the field contiguous to this source / drain field whose part or gate electrode of an extended field is pinched between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field.

[0027] In this invention, through the low high-impurity-concentration field of the source / drain field lower part, or th low high-impurity-concentration field of the width, an electron hole reaches an extension and is eliminated from th field which introduced the second conductivity-type impurity into high concentration by the above-mentioned composition.

[0028] The first above-mentioned technical problem in the conventional technology is p+ which passed the electron hole in the direction of channel width in the gate lower part, and was prepared in contact with the channel formation field (semiconductor region of the gate electrode lower part). It leads to a type field and is p+. From a type field, it originates in the structure of eliminating an electron hole, and generates.

[0029] On the other hand, p+ which passes an electron hole in the perpendicular direction to the direction of channel width in a low high-impurity-concentration field, and adjoins a low high-impurity-concentration field in this invention The electron hole is eliminated from the field. Since it becomes a path for the low high-impurity-concentration field of the source / drain field lower part or the low high-impurity-concentration field of the width passing an electron hole in the perpendicular direction to the direction of channel width, a channel formation field is touched, and it is p+. It is not necessary to prepare a type field. Therefore, p+ By preparing a field, the problem whose efficiency-channel width decreases can be solved or suppressed, and the first technical problem is canceled or suppressed.

[0030] An impurity does not have the field (low high-impurity-concentration band) introduced into low concentration in the field which adjoined the source / drain field on both sides of the gate electrode especially, but in a part of this xtended field, when high impurity concentration prepares a low field, there is no efficiency-reduction of channel width between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field.

[0031] Moreover, it also sets, when establishing the field (low high-impurity-concentration band) which introduced the impurity into low concentration in the field which adjoined the source / drain field on both sides of the gate electrode, and it is p+. Since the width of face can be narrowed compared with the case where adjoin a gate electrode and a field is prepared, efficiency-reduction of channel width can be suppressed.

[0032] The reason is as follows. p+ When a gate electrode is adjoined and it prepares a field, it is necessary to prepare the contact field linked to wiring into it. Therefore, p+ in the conventional technology Only the width of face of contact and the width of face containing the fixed margin surrounding it are needed, and, as for a field, bigger width of face than width of face indispensable for exclusion of an electron hole is needed. In the structure of this invention, since the contact for eliminating an electron hole is taken to the extended field distant from the gate, it is not generated but this problem can make small width of face of the field which introduced the impurity contiguous to this source / drain field into low concentration.

[0033] Moreover, since the low low high-impurity-concentration band of high impurity concentration and an extension are between the field which introduced the second conductivity-type impurity into high concentration, and the source / drain field and a depletion layer is formed in these fields, it is p+. Electric field are eased by the depletion layer between a field and n field, and the flow by the tunnel between bands is barred. Therefore, p+ A field is prevented from the potential of n field being interlocked with.

[0034] Therefore, it is p+ even if the field which introduced the second conductivity-type impurity into high concentration is in a drain side. Since the potential of a field does not rise, the leakage current does not flow. Since the field which introduced the second conductivity-type impurity into high concentration can be established in a drain side and symmetrical structure is acquired, the second above-mentioned technical problem resulting from unsymmetrical structure is solved. Moreover, since a field screening electrode is not prepared, the third and the fourth technical problem are solved. Moreover, since body contact sees from the source / drain field and there is in the direction of channel width, the fifth technical problem is solved.

[0035] Moreover, in the state where grounding potential is given to the source / drain field, the high impurity concentration of the second conductivity type of the source / drain field lower part is low set up so that all the lower parts of the source / drain field may become a depletion layer.

[0036] Th n, under the sourc / drain field, a depletion layer reaches the bottom of a SOI layer. Thereby, since th parasitic capacitance of the drain fi ld lower part decreases, a working spe d improves. Moreover, since the potential of a depletion layer is lower than the source / drain field, the depl tion layer of the sourc field low r part can mak it become the path of an electron hole, although an electron hole flows th low place of potential.

[0037] Moreover, when the voltage used as the threshold in which a channel is form d is appli d to a gate electrode, the high impurity concentration of a semiconductor layer is set up so that all the semiconductor layers located in

the gate electrode lower part may turn into a depletion layer. If all become [th semiconductor layer located in the gate electrode lower part] a depletion layer, it will be hard coming to accumulate an l ctron hole (if a perfect depletion is formed). This reduces th burden about the exclusion capacity of an electron hole, and is a book.
[0038] this invention touches a gate lectrode and is p+. A field is not prepar d, but it l ts the low fi ld of high impurity concentration pass, and is an electron hole p+ It leads to a field. The low field of high impurity concentration is p+. Although the capacity to pass an electron hole compar d with a field is inferior, the problem that the capacity to pass an electron hole is inferior can be offset by r ducing accumulation of an electron hol by perfect depletion-ization.
[0039] Moreover, it does not have the field which introduced the impurity into low concentration in the field which adjoined the source / drain field on both sides of the gate electrode, but high impurity concentration prepares a low field in a part of this extended field between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field.
[0040] Also in this case, since an electron hole can be discharged via the bottom of the source/drain, the second above-mentioned technical problem is solvable.
[0041] Moreover, the second conductivity-type impurity prepared in a part of extended field is connectable with the semiconductor layer or conductor layer under an oxide film. It is not necessary to prepare the body contact which met with wiring in contact with the transistor, and the seventh above-mentioned technical problem can be solved.
[0042] Moreover, the source / drain field is formed from an epitaxial layer, a low concentration field is established in the bottom of it, and if a low concentration field is connected to the high high-impurity-concentration field of the second conductivity type in the field distant from the source / drain field, since the source/drain will become a single crystal, the sixth above-mentioned technical problem is solved.
[0043] Moreover, the second conductivity-type field of high high impurity concentration is not established in an extended field, but a metal is directly contacted to an extension.
[0044] Moreover, the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode is adjoined, and an insulator layer thicker than the gate insulator layer of other fields is prepared between a gate lectrode and the semiconductor layer located in the bottom of it in the field located in the gate electrode lower part at a semiconductor layer. Or the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode is adjoined, and concentration of the second conductivity-type impurity is made higher than other fields under a gate electrode in the semiconductor layer located in the gate electrode lower part.
[0045] By these, the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode is adjoined, threshold voltage of the field located in the gate electrode lower part at a semiconductor layer is made high, and formation of a channel can be suppressed. A channel becomes the low high-impurity-concentration band 21 is hard to be formed, and the capacity between gate-channels stops then, attaching to this portion. The problem relevant to the first above-mentioned technical problem that the effective width of the source / drain field decreases by this, without the capacity between gate-channels becoming less is mitigated.
[0046] Moreover, it is made for wiring linked to the source to be located on the insulator layer on the field which is prepared in the field contiguous to this source / drain field whose part or gate electrode of this extended field is pinched and where high impurity concentration is low.
[0047] Or it is made for the wiring which connected this second conductivity-type impurity to the upper part of these fields to the field introduced into high concentration to be located.
[0048] If these fields are covered by the wiring which connected the wiring or this second conductivity-type impurity linked to the source to the field introduced into high concentration, these low high-impurity-concentration fields will become lower than grounding potential (or potential of wiring). Since an electron hole flows the low place of potential, an electron hole becomes easy to flow to these fields.
[0049]
[Embodiments of the Invention] Hereafter, the form of operation of this invention is described, referring to a drawing.

[0050] The plan of the field effect transistor based on this invention is shown in drawing 1 about the case of an n channel transistor. A1-A1'cross-section and B1-B1' the cross section of drawing 1 is shown in drawing 2 and drawing 3 , respectively.
[0051] The gate electrode 4 is formed on the semiconductor layer 2 on an oxide film 11. Setting in the semiconductor layer 2 whose gate electrode 4 is pinched, the upper part is n+. It is p which diffused the impurity of concentration with the low lower part of nothing and the semiconductor layer 2 for the type source drain field 5. - A field 26 is made. The gate insulator layer 3 is formed in the lower part of the gate electrode 4, and the semiconductor layer 2 of the lower part of a gate electrode makes the channel formation field 27. It connects with the wiring which the source / drain contact 23 is formed on the source / drain field 5, and consists of aluminum 24. in order [however,] to make element structure intelligible — aluminum 24 — the drawing 3 **** — only — it is shown
[0052] Th low high-impurity-concentration band 21 of the semiconductor layer 2 with which the source / drain field 5 was established in neither in a s miconductor layer and on a lay r in the fi ld, but th impurity was introduced into low conc ntration is made in part. The xt nded field 7 which furthermore projected from the low high-impurity-concentration band 21 in th direction of channel width is form d. However, a direction parallel to the source / drain field, and the boundary of a gate electrode is called dir ction of channel width here. p+ which introduced p typ impurity into a part of extended field [at least] 7 at high concentration A fi ld 8 is formed, th

body contact 9 is formed in p field, and it connects with the wiring which consists of aluminum 24. The wiring connected to the body contact 9 maintains grounding potential, or if it is potential [at least] smaller than th band gap of a semiconductor layer, for example, silicon, it will maintain the pot ntial not more than 1.12V. The pot ntial of the wiring connected to body contact is grounded, or when it is negative, th electron hole exclusion capacity of body contact becomes high. However, a certain amount of exclusion capacity is acquired as potential is higher than grounding potential. However, if it becomes higher than the potential quivalent to a band gap, since th leakage current from body contact to th source will b com r markable, this ne ds to avoid.

[0053] The electron hole generated in the channel section in this structure is p+ formed in the extended field 7 through the low concentration field 26 and the low high-impurity-concentration band 21 of the source / drain field lower part. It flows into a field 8 and can eliminate through the body contact 9. Therefore, the electron hole leading to the substrate suspension effect will be eliminated.

[0054] The first technical problem (fall of efficiency-channel width) in the conventional technology passes an electron hole in the direction of channel width in the gate lower part, and is p+. p+ which led to the field and was prepared in contact with the channel formation field (semiconductor region of the gate electrode lower part) From a type field, it originates in the structure of eliminating an electron hole, and generates.

[0055] On the other hand, p+ which passes an electron hole in the perpendicular direction to the direction of channel width in a low high-impurity-concentration field (21 26), and adjoins a low high-impurity-concentration field in this invention An electron hole is eliminated from a field 8. Since it becomes a path for the low high-impurity-concentration field 26 of the source / drain field lower part or the low high-impurity-concentration field 21 of the width passing an electron hole in the perpendicular direction to the direction of channel width, a channel formation field is touched, and it is p+. It is not necessary to prepare a type field. Therefore, p+ By preparing a field, the problem that efficiency-channel width falls can be solved or suppressed, and the first above-mentioned technical problem is solved.

[0056] It does not have the low high-impurity-concentration band 21 especially, but they are the source / drain field, and p+. The low concentration field 32 is formed between fields, and there is no efficiency-reduction of channel width with the structure (drawing 13 and its B13-B13' cross section, drawing 14) which has the low concentration field 26 under the source / drain field. Moreover, it also sets, when forming the low high-impurity-concentration band 21, and it is p+. Since width of face of the low high-impurity-concentration band 21 can be narrowed compared with the case where adjoin a gate electrode and a field is prepared, efficiency-reduction of channel width can be suppressed.

[0057] The reason is as follows. It is p+ like the conventional example (25 drawing 24 , 26). When a gate electrode is adjoined and it forms a field 105, it is necessary to prepare the contact field linked to wiring into it. Therefore, p+ in the conventional technology Only the width of face of contact and the width of face containing the fixed margin surrounding it are needed, and, as for a field, bigger width of face than width of face indispensable for exclusion of an electron hole is needed. In the structure of this invention, since the contact for eliminating an electron hole is taken to the extended field 7 distant from the gate, width of face of the low high-impurity-concentration band 21 can be made small, and the first above-mentioned technical problem can be suppressed.

[0058] p+ Since it is isolated by the low high-impurity-concentration band 21 or the p field 32, there is no mutual flow of a field 8, and five the source / drain field. That is, the field strength between both is eased by isolating both (p+ field, and the source/drain). Therefore, when a drain becomes high potential, it can prevent strong electric field's becoming a cause and the tunnel current between bands flowing among both. Therefore, p+ Even if a field is in a drain side, a drain and the leakage current during body contact do not flow. Therefore, body contact can be prepared in both the source / drain field, and the second above-mentioned technical problem (asymmetry) can be solved.

[0059] Moreover, it is p+ like drawing 24 and the conventional example of 26. A field is touched, and since it is not necessary to prepare the semiconductor layer located under the gate as a path of an electron hole, the parasitic capacitance between a gate electrode and its semiconductor layer is not attached. Moreover, since a field screening electrode like the conventional example of drawing 27 is not prepared, the above-mentioned third and the fourth technical problem are solvable.

[0060] Moreover, since body contact is prepared in the portion extended in the direction of channel width from the source / drain field, it is applicable also to the connected structure in which the gate array etc. carried out transistor continuation. Therefore, the fifth above-mentioned technical problem is solved.

[0061] Hereafter, the gestalt of other operations is described.

[0062] In the state where grounding potential is given to the source / drain field, the high impurity concentration of the second conductivity type of the source / drain field lower part can be low set up so that all the lower parts of the first conductivity-type source / drain field may become a depletion layer.

[0063] Then, under the source / drain field, a depletion layer reaches the bottom of a SOI layer. Thereby, since th parasitic capacitance of the drain field lower part decreases, a working speed improves. Moreover, although an electron hole flows time with the low of potential, rather than the source / drain field, it is a low and, as for the potential of a depletion lay r, th d pletion layer of th source field lower part is made as for a bird clapper to the path of an electron hole.

[0064] Moreov r, when the voltag us d as the threshold in which a channel is form d is applied to a gate l ctrode, the high impurity concentration of a semiconductor layer can b set up so that all the semiconductor lay rs locat d in the gate electrode lower part may turn into a depletion layer. ** for which an electron hole stops being able to accumulate easily since the potential of the field will go up, if all become [the semiconductor layer located in the

gate electrode lower part] a depletion layer. This reduces the burden about the exclusion capacity of an electron hole, and is a book.
[0065] this invention touch s a gat electrode and is p+. A field is not prepared, but it lets the low field of high impurity concentration pass, and is an electron hole p+ It leads to a field. The low field of high impurity concentration is p+. Although th capacity to pass an electron hole compared with a field is inferior, the problem that the capacity to pass an electron hole is inferior can be offset by r ducing accumulation of an electron hol by p rfect depletion-ization.
[0066] Moreover, drawing 4 , and 5, 6 and 7 are p+. It is explanatory drawing of the gestalt of operation of this invention in case it does not connect with wiring 24 but a field 8 is connected with a silicon substrate 10 by the body plug 15, and, for drawing 4 and drawing 5 , the body plug 15 is p+. When piercing through a field, drawing 6 and drawing 7 are p+. It is the case where it touches from the side without piercing through a field. For drawing 8 , the body plug 15 is p+. It is the case where a field 8 is touched from the bottom.
[0067] p+ Since it connects with silicon machine 10 boards [directly under] of it and an electron hole is discharged by the silicon substrate 10, a field 8 is p+. It is not necessary to make the wiring which connects a field and a grounding conductor. Moreover, it embeds into the portion which touches the body plug 15 at a silicon substrate 10, and is p+. The case where a field 28 is formed is shown in drawing 9 and drawing 10 . It embeds at a silicon substrate 10 and is p+. If a field is prepared, a flow of the electron hole in a silicon substrate will be improved.
[0068] The case where the source / drain field is formed by the epitaxial layer 30 in the structure of drawing 1 is shown in drawing 11 . By diffusing Lynn from an epitaxial layer shallowly, it is n+ to the front face of a semiconductor layer. A field 31 is formed shallowly.
[0069] In drawing 1 , the case where the low high-impurity-concentration band 21 is not formed is shown in drawing 13 and drawing 14 . In this case, it is p to the portion which touches the source / drain field among the extended fields 7. - A field 32 is formed. In this case, p in the extended field 7 - A field 32 replaces the low high-impurity-concentration band 21, and is p+. It has the operation which eases the electric field between a field, and the source / drain field 5. Moreover, p in the low high-impurity-concentration band 21 and the extended field 7 - You may form both fields 32.
[0070] Moreover, the cross section in B1-B1' in case the source / drain field 5 reaches the background of the semiconductor layer 2 is shown in drawing 15 by the case where the low high-impurity-concentration band 21 is formed. In this case, after an electron hole flows the channel field under a gate electrode in the direction of channel width and reaches the low high-impurity-concentration band 21, it is discharged from the extended field 7. In this case, since the source / drain field may arrive at the bottom of a SOI layer, it is not necessary to formation of the source / drain field to form shallow junction.
[0071] Moreover, it sets in the structure of drawing 13 and is p+ to an extension. A field is not prepared, but a metal is contacted directly and the case where Schottky contact (connection of wiring 24 and the low concentration layer 21) is taken is shown in drawing 17 . In this case, you may use a tungsten, tungsten silicide, etc. for wiring. Moreover, in order to adjust the size of the Schottky barrier, you may also insert metals, such as TiN and tungsten silicide, or the compound containing a metallic element as an interlayer between the low concentration layer 21 and wiring 24. In this case, Schottky contact is formed of the low concentration layer 21 and an interlayer.
[0072] The Schottky contact in which the metal was contacted has a rectifying action in a low-concentration semiconductor layer. The band view in the case (in the low case [The potential by the side of a metal]) of grounding the metal which forms Schottky contact is shown in drawing 32 . Although a surplus electron hole can flow to a metal side, an electron cannot flow because of the obstruction formed in the semiconductor layer (p-field) of low concentration [side / channel / side / metal]. Moreover, the case where the potential by the side of a metal is high is shown in drawing 33 and drawing 34 . If a metal is contacted to high p substrate of p type high impurity concentration, since it will become like drawing 33 , a thin obstruction will be formed in the field in which a depletion layer is formed in p substrate in contact with a metal and an electron hole will pass through this obstruction according to a tunnel phenomenon, an excessive hole current will be poured in from a metal side. On the other hand, a metal is low-concentration p like this invention. - The case where a field or the intrinsic (i) field is contacted is shown in drawing 34 . In this case, since a low concentration field and i field are influenced of drain voltage and become the voltage near drain potential, the obstruction over an electron hole is formed like drawing 34 , and an electron hole is not poured in. Since the field influenced of drain electric field serves as an obstruction as shown in drawing 34 when a low concentration field connects this to a channel through the low concentration field under a drain like especially drawing 13 , it is remarkable ineffective.
[0073] Moreover, drawing 18 shows the state where the structure of drawing 1 was connected when two or more transistors, such as a gate array, were connected and had been arranged, and drawing 19 is p+. A field 8 is extended and the example which formed the body contact 9 outside the contact 22 to a gate electrode is shown. Like drawing 18 , body contact is p+. You may open so that a field may be covered. (The margin of p+ field which surrounds contact is not taken) .
[0074] Moreov r, in a gate array, th sourc of each oth r is connected with body contact in the electrode used as th source. It sets to th fi ld us d as a drain, and is p+. It is made not to open a contact hole in th field upper part. This s ts to the field used as a drain, and it is p+. It also s ts to any wh n not passing, when the wiring which connects the field upper part to a drain passes, and is p+. It can prev nt a field and a drain electrode short-circuiting electrically.
[0075] When it is not decided like the transfer gate any shall be on a high-voltage side between the sourc / drain

field, body contact is not connected with the source / drain field, but all body contacts are grounded. That is, it connects with wiring with grounding potential.
[0076] Moreover, the low concentration field of the source / drain field lower part is n to drawing 20 . – Th case where it is type is shown.
[0077] p– When a silicon substrat is grounded, it is p from the relation of a work function. – A substrate serves as low potential from the source. Moreover, ven if it gives an el ctronegative potential to a silicon substrat , a silicon substrate serves as low potential from the source similarly. Then, even if it establishes n–field in the bottom of the source / drain field, a depletion layer is formed in this field of the influence of the electric field from a substrat . if a depletion layer is formed — n– n type with which polarity differs from an electron hole since the potential of a field 40 falls — it is also — it does not start but an electron hole becomes easy to flow
[0078] Drawing 21 shows the case where the oxide film on the field (channel field contiguous to a low high–impurity–concentration band) inserted into the low high–impurity–concentration band 21 is made thicker than a gate oxide film (the middle insulator layer 41 of drawing 21 and drawing 21 are equivalent to the D1–D1' cross section of drawing 1). If the middle insulator layer 41 is formed, the threshold voltage of this portion will go up. If this has a thick gate oxide film, it will be based on the principle that threshold voltage goes up. A channel becomes is hard to be formed in the field contiguous to the low high–impurity–concentration band 21, and the capacity between gate channels (gate capacitance) stops then, attaching to this portion.
[0079] Thereby, the influence of the effective width of the source / drain field decreasing can be reduced by forming the low high–impurity–concentration band 21. Although it is disadvantageous, if the effective width of the source / drain field decreases without the capacity between gate–channels becoming less, and the capacity between gate–channels becomes less with the effective width of the source / drain field to a working speed, the demerit over a working speed can be reduced.
[0080] Moreover, the middle insulator layer 41 may cover the low high–impurity–concentration band 21 top. In this case, the effect that the capacitive component between a low high–impurity–concentration band and the wiring arranged on it is mitigable is acquired.
[0081] Moreover, if p type high–impurity–concentration band of a low high–impurity–concentration band is increased, since the threshold voltage of this portion will go up and a channel will no longer be formed, the source / drain field can mitigate the problem that capacity is attached in the portion (portion pinched by the low high–impurity–concentration band 21) which does not work effectively, also by this method.
[0082] Moreover, the low high–impurity–concentration band 21 or the low high–impurity–concentration field 32 of an xtension can be covered with the wiring 42 linked to body contact. If p type impurity is introduced into the low high–impurity–concentration band 21 or the low high–impurity–concentration field 32 of an extension, potential will become low rather than the wiring which these fields have in the upper part. If grounding potential has body contact, these low high–impurity–concentration fields (21 32) will become lower than grounding potential. Since an electron hole flows the low place of potential, an electron hole becomes easy to flow to these fields (21 32).
[0083] Moreover, the example which covered the low high–impurity–concentration band 21 or the low high–impurity–concentration field 32 of an extension with the wiring 43 linked to the source / drain field in the structure of drawing 13 is shown in drawing 23 . As for a source side, although either the source or a drain field operate as the source, since potential is low, like the case where it covers by the result above–mentioned grounding conductor, an electron hole becomes easy to flow to a low high–impurity–concentration field by the source side, and an electron hole becomes is easy to be eliminated.
[0084]
[Example]
The plan of the field effect transistor based on this example is shown in example 1 drawing 1 . A1–A1'cross–section and B1–B1' the cross section of drawing 1 is shown in drawing 2 and drawing 3 , respectively.
[0085] It is n+ so that the semiconductor layer 2 may be crossed on the semiconductor layer 2 on an oxide film 11. The gate electrode 4 with a width of face of 0.25 microns which consists of contest polysilicon is formed. The gate insulator layer 3 with a thickness of 5nm is formed in the lower part of the gate electrode 4. It is p to which the lower part of nothing and the semiconductor layer 2 diffused the p type impurity for the source drain field 5 where the upper part diffused the n type impurity in high concentration to low concentration in the semiconductor layer 2 whose gate electrode 4 is pinched. – A field 26 is made. The semiconductor layer 2 of the lower part of a gate electrode makes the channel formation field 27 in which a channel is formed. It connects with the wiring which the source / drain contact 23 is formed on the source / drain field 5, and consists of aluminum 24.
[0086] The source / drain field 5 is not formed, but a part of semiconductor layer 2 is p. – The low high–impurity–concentration band 21 of type is made. The extended field 7 which furthermore projected from the low high–impurity–concentration band 21 in the direction of channel width is formed. However, a direction parallel to the source / drain field, and the boundary of a gate electrode is called direction of channel width here. p+ which introduc d p type impurity into a part of extended field [at least] 7 at high concentration A field 8 is formed and it is p+. Th body contact 9 is formed in a field and it connects with th wiring which consists of aluminum 24. The wiring connected to the body contact 9 maintains grounding potential, or if it is potential [at l ast] smaller than the band gap of a semiconductor layer, for example, silicon, it will maintain th potential not mor than 1.12V.
[0087] In the cross section of drawing 2 and drawing 3 , in 10, a silicon substrate and 11 show an embedding oxid film, and 25 shows a layer insulation film. Thickness of an embedding oxide film and a lay r insulation film was set to 400nm, respectively. Width of face [as opposed to the direction of chann l width of 1 micron, and the source / drain

field in width of face / as opposed to th direction of channel width of 20nm and the low high-impurity-concentration band 21 in the thickness of 60nm, and the sourc / drain field 5] made SOI layer thickness 10 microns. Width of face of a direction parallel to the direction of A1-A1' of an ext nded field was made into 0.3 microns. p- For boron, in a field 26, boron is 1x1017cm-3 and p+ to 1x1017cm-3 and the low high-impurity-concentration band 21. Boron was introduced into the field 8 and Lynn was introduced into 1x1019cm-3, and the source / drain field 1x1019cm-3. A silicon substrate is p containing th boron of concentration 1x1016cm-3. - It considered as type.

[0088] The electron hole generated in the channel section in this structure is p+ formed in the ext nded field 7 through the low concentration field 26 and the low high-impurity-concentration band 21 of the source / drain field lower part. It flows into a field 8 and can eliminate through the body contact 9. Therefore, the electron hole leading to the substrate suspension effect will be eliminated.

[0089] p+ Since it is isolated with the low high-impurity-concentration band 21, there is no mutual flow of a field 8, and five the source / drain field. That is, it also sets not only to the source but to a drain field, and is p+. The leakage current does not flow with the tunnel between bands etc. between fields. Therefore, body contact can be symmetrically prepared in both the source / drain field. Moreover, there is no reduction of the effective channel width accompanying formation of body contact. Moreover, since the source / drain field prepares body contact in the portion extended in the direction of channel width, it is applicable also to the structure which transistors, such as a gate array, connected continuously.

[0090] It sets to drawing 1 and example 2 this example is p+. It is the case where do not connect with wiring but the field 8 is connected with the silicon substrate 10.

[0091] For drawing 4 and drawing 6 , this example is p+, respectively. The plan and drawing 5 which expanded the field 8 neighborhood, and drawing 7 are C4-C4' in drawing 4 and drawing 6 , and an elevation in a C6-C6' cross section, respectively. It also sets to any and is p+. A field 8 is p+. It is p by the body plug 15 which consists of contest polysilicon. - It connects with the silicon substrate 10. Drawing 4 and drawing 5 are p+. When piercing through a field, drawing 6 and drawing 7 are p+. It is the case where it touches from the side without piercing through a field. For drawing 8 , a body plug is p+. It is the case where it touches from under a field. p+ Since a field is connected to the silicon substrate [directly under] of it and an electron hole flows into a silicon substrate, it is p+. It is not necessary to make the wiring which connects a field and a grounding conductor.

[0092] Moreover, it embeds into the portion which touches the body plug 15 at a silicon substrate 10 as shown in drawing 9 and drawing 10 , and is p+. You may form a field 28. p+ A field 28 is second p+ which pierces through an embedding oxide film in the position distant from the transistor. It connects with a grounding conductor with the wiring which consists of a polysilicon contest plug 29 and aluminum 24 (drawing 9). Moreover, you may use a metal like aluminum 24 as a material of a plug (drawing 10). It embeds at a silicon substrate 10 and is p+. When the field was prepared, the flow of the electron hole in a silicon substrate was able to be improved. The body plug 15 is formed by performing embedding by CVD of plug material (conductors, such as contest p+ polysilicon, a metal, and metal silicide) etc., and etchback by continuing RIE.

[0093] Example 3 this example shows the cross section of this example to drawing 11 about the A1-A1' cross section of drawing 1 in the structure of drawing 1 by the case where the source / drain field is formed by the epitaxial layer 30. High-concentration Lynn was introduced into the epitaxial layer 30. It is n+ to the front face of a semiconductor layer by diffusing Lynn from an epitaxial layer shallowly with heat treatment by lamp annealing or the electric furnace. The field 31 was formed shallowly. n+ The thickness of a field 31 is 20nm.

[0094] Drawing 13 shows a plan and the B13-B13' cross section of drawing 13 to drawing 14 by the case where example 4 this example does not form the low high-impurity-concentration band 21 in drawing 1 . p which introduced boron into the portion which touches the source / drain field among the extended fields 7 in this structure low concentration 1x1017cm-3 - The field 32 was formed. In this case, the p-field 32 in the extended field 7 replaces the low high-impurity-concentration band 21, and is p+. It has the operation which eases the electric field between a field, and the source / drain field 5. Moreover, p in the low high-impurity-concentration band 21 and the extended field 7 - You may form both fields 32.

[0095] When forming the example 5 low high-impurity-concentration band 21, the source / drain field 5 may reach the background of the semiconductor layer 2. this example is an example in this case, and shows the cross section in that case to drawing 15 (setting in the position equivalent to the B1-B1' cross section of drawing 1). In this case, after an electron hole passes along the channel field under a gate electrode and reaches the low high-impurity-concentration band 21, it is discharged from the extended field 7. In this case, since the source / drain field may arrive at the bottom of a SOI layer, it is not necessary to form shallow junction and there is a merit that the usual ion implantation etc. can use the existing process, to formation of the source / drain field (drawing 15).

[0096] It sets in the structure of drawing 13 and example 6 this example is p+ to an extension. A field is not prepared, but a metal is contacted directly and the B13-B13' cross section in drawing 13 is shown in drawing 17 by th case where Schottky contact is taken. Moreover, the same cross section shows the case where Schottky contact is connected with th contact on the source / drain field to drawing 16 .

[0097] The Schottky contact in which the metal was contacted has a r ctifying action in a low-conc ntration semiconductor layer. The band view in the case (when the potential by the side of a m tal is low) of grounding th metal which forms Schottky contact is shown in drawing 32 . Although a surplus electron hole can flow to a m tal side, an electron cannot flow because of the obstruction formed in th semiconductor layer (p-field) of low concentration [side / channel / side / metal]. Moreover, the case wher the potential by the side of a m tal is high

is shown in drawing 33 and drawing 34 . If a metal is contacted to high p substrate of p type high impurity concentration, since it will becom like drawing 33 , a thin obstruction will be form d in the field in which a depletion layer is formed in p substrate in contact with a metal and an lectron hole will pass through this obstruction according to a tunnel phenomenon, an excessive hole current will be poured in from a metal side. On the oth r hand, a metal is low-concentration p like this invention. - The case where a field or the intrinsic (i) fi ld is contacted is shown in drawing 34 . In this cas , since a low concentration field and i field are influenc d of drain voltage and become the voltage near drain potential, the obstruction over an lectron hole is formed like drawing 34 , and an electron hole is not poured in. Since the field influenced of drain electric field serves as an obstruction as shown in drawing 34 when a low concentration field connects this to a channel through the low concentration field under a drain like especially drawing 13 , it is remarkable ineffective.

[0098] Moreover, it enables this to connect the source / drain field, and body contact like drawing 16 . That is, when the source / drain field acts as the source with low potential, while an electron hole is eliminated through this, when acting as a drain with high potential, a leakage current does not occur, but symmetrical structure becomes possible.

[0099] Moreover, you may use a tungsten, tungsten silicide, etc. for wiring. Moreover, in order to adjust the size of the Schottky barrier, you may also insert metals, such as TiN and tungsten silicide, or the compound containing a metallic element as an interlayer between the low concentration layer 21 and wiring 24.

[0100] Example 7 this example is [the example (drawing 18 ; plan) which connected the structure of drawing 1 when two or more transistors, such as a gate array, were connected and it had been arranged, and] p+. It is an xample (drawing 19 ; plan) in case a field 8 is extended and body contact is prepared outside the contact to a gate lectrode. Body contact is p+. The source of each other is connected with body contact in the electrode from which it can open so that a field may be covered (the margin of p+ field which surrounds contact is not taken), and ** also s rves as the source in a good (drawing 18) gate array. It sets to the field used as a drain, and is p+. It is made not to open a contact hole in the field upper part. This sets to the field used as a drain, and it is p+. It also sets to any when not passing, when the wiring which connects the field upper part to a drain passes, and is p+. It can prevent a field and a drain electrode short-circuiting electrically.

[0101] When it is not decided like the transfer gate any shall be on a high-voltage side between the source / drain field, body contact is not connected with the source / drain field, but all body contacts are grounded, namely, are connected to wiring with grounding potential.

[0102] For example 8 this example, the low concentration field of the source / drain field lower part is n. - By the case where it is type, the cross section is shown in drawing 20 (setting in the position equivalent to the B1-B1' cross section of drawing 1). The lower part of the source / drain field is poured-in n 1x1017cm-3 about Lynn. - It considered as the field 40. A silicon substrate 10 is p. - It considered as type. It considered as grounding potential (0V) or the electronegative potential at the silicon substrate 10.

[0103] p- When a silicon substrate is grounded, it is p from the relation of a work function. - A substrate serves as potential lower than the source. Moreover, p - It is p when an electronegative potential is given to a silicon substrate. - It becomes low potential. Then, it is n under the source / drain field. - Even if it prepares a field, a depletion layer is formed in this field in response to the influence of the potential of a silicon substrate. if a depletion layer is formed -- n- n type with which polarity differs from an electron hole since the potential of a field falls -- it is also -- it does not start but an electron hole becomes easy to flow

[0104] Example 9 this example is an example at the time of making the oxide film on the channel formation field contiguous to the low high-impurity-concentration band 21 thicker than a gate oxide film.

[0105] In drawing 1 , the D1-D1' cross section at the time of forming the middle insulator layer 41 on the channel formation field (field under a gate electrode) which adjoins the low high-impurity-concentration band 21 and it is shown in drawing 21 .

[0106] If the middle insulator layer 41 is formed, the threshold voltage of this portion will go up. If this has a thick gate oxide film, it will be based on the principle that threshold voltage goes up. A channel becomes the low high-impurity-concentration band 21 is hard to be formed, and the capacity between gate-channels stops then, attaching to this portion.

[0107] Thereby, the influence of the effective width of the source / drain field decreasing can be reduced by forming the low high-impurity-concentration band 21. Although it is disadvantageous, if the effective width of the source / drain field decreases without the capacity between gate-channels becoming less, and the capacity between gate-channels becomes less with the effective width of the source / drain field to a working speed, the demerit over a working speed can be reduced.

[0108] Moreover, if p type high impurity concentration of a low high-impurity-concentration band is increased, since the threshold voltage of this portion will go up and a channel will no longer be formed, the source / drain field can mitigate the gate capacitance to the portion which does not work effectively also by this method.

[0109] In example 10 this example, the example which covered the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension with the wiring 42 linked to body contact in the structure of drawing 1 is shown in drawing 22 (plan).

[0110] If p type impurity is introduc d into th low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension, potential will become low rather than the wiring which these fields have in the upper part. If grounding potential has body contact, th se low high-impurity-concentration fields will become lower than grounding potential. Since an electron hole flows the low place of potential, an electron hole b comes easy to flow to these fields.

[0111] Moreover, the exampl which covered the low high-impurity-concentration band 21 or th low high-impurity-concentration field 32 of an extension with the wiring 43 linked to the sourc / drain field in th structure of drawing 13 is shown in drawing 23 (plan).
[0112] As for a source side, although either the source or a drain field operate as the sourc , potential is a low, as a result, like the upper case, an electron hole becomes easy to flow to a low high-impurity-concentration field (21 32) by the source side, and an electron hole becomes is easy to be liminated.
[0113] As mentioned abov , although the example about an n channel transistor was shown, in the cas of a p-channel transistor, all polarity should just be made into reverse in the above example.
[0114]
[Effect of the Invention] The electron hole generated in the channel section in the structure of the electric-field type transistor of this invention is p+ formed in the extended field 27 through the low concentration field 26 and the low high-impurity-concentration band 21 of the source / drain field lower part. It flows into a field 8 and can eliminate through the body contact 9. Therefore, the electron hole leading to the substrate suspension effect is liminated.
[0115] p+ Since it is isolated by the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension, there is no mutual flow of a field 8, and five the source / drain field. That is, it also sets not only to the source but to a drain field, and is p+. The leakage current does not flow with the tunnel between bands . tc. between fields. Therefore, body contact can be symmetrically prepared in the source / drain field of both sides.
[0116] Moreover, since it is not necessary to prepare the semiconductor layer used as the path of an electron hole in the bottom of the gate, the parasitic capacitance between a gate electrode and its semiconductor layer is not attached. Moreover, since body contact is prepared in the portion which extended the source / drain field in the direction of channel width, it is applicable also to the structure which transistors, such as a gate array, connected continuously.
[0117] Moreover, it is p+ by the body plug. It is p+ when a field and the silicon substrate [directly under] of it are connected. It is not necessary to make the wiring which connects a field and a grounding conductor. Furthermore, it is p+. It embeds at the silicon substrate 10 connected with a field, and is p+. If a field is prepared, a flow of the electron hole in a silicon substrate can be improved.
[0118] Moreover, with the structure of passing an electron hole, the low high-impurity-concentration band 21 is not formed, but the field which introduced the impurity into the portion which touches the source / drain field among the extended fields 7 at low concentration is established in the bottom of the source / drain field. Then, the low concentration field in an extended field is p+. It has the operation which eases the electric field between a field, and the source / drain field 5. If electric field are eased, the tunnel current between bands will decrease and the leakage current will be suppressed.
[0119] Moreover, when forming the low high-impurity-concentration band 21 in some fields of the direction of channel width, the source / drain field 5 may reach the background of the semiconductor layer 2. In this case, from the channel field under a gate electrode, after an electron hole reaches the low high-impurity-concentration band 21, it is discharged from the extended field 7. In this case, since the source / drain field may arrive at the bottom of a SOI layer, it is not necessary to form shallow junction and the usual ion implantation etc. has the merit that the existing process can be used, to formation of the source / drain field.
[0120] Moreover, it is p+ to an extension 7. While the rectifying action will protect that a surplus charge flows from the metal section even if the metal section serves as high potential if a field is not prepared, but a metal is contacted directly and Schottky contact is taken, an electron hole [surplus / in a SOI layer] can be eliminated.
[0121] Moreover, the source of each other is connected with body contact in the electrode used as the source. It sets to the field used as a drain, and is p+. It is made not to open a contact hole in the field upper part. It sets to the field which serves as a drain by this while being able to simplify wiring, and is p+. It also sets to any when not passing, when the wiring which connects the field upper part to a drain passes, and is p+. It can prevent a field and a drain electrode short-circuiting electrically.
[0122] if low-concentration n type field is established in the lower part of the source / drain field and the silicon substrate under an embedding oxide film is made into grounding potential (0V) or an electronegative potential in an n channel electric field effect type transistor — n- under the source / drain field n type with which a depletion layer is formed in a field and polarity differs from an electron hole — it is also — it does not start but an electron hole becomes easy to flow
[0123] In the first conductivity-type electric field effect type transistor, the middle insulator layer 21 is formed in the middle of a semiconductor layer and a gate electrode in the field to which the source / drain field is not adjoined, and a semiconductor layer is located in the lower part of a gate electrode. Or the concentration of the second conductivity-type impurity of the semiconductor layer of this field is raised. Since the threshold voltage in the semiconductor layer of this portion goes up, the capacity between gate-channels stops then, attaching to this portion. The demerit in the working speed by the effective width of the source / drain field decreasing by this can be reduc d.
[0124] The source / drain field, and p+ Th high impurity concentration located in the middl of a field covers with the wiring which connects a low field (the low high-impurity-concentration band 21 or low high-impurity-concentration field 32 of an extension) to the wiring or th sourc link d to body contact. Then, an electron hole becomes easy to flow to these fi lds, and exclusion of a SOI layer to an electron hol becomes easy.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the SOI transistor formed especially on an insulator about the field effect transistor used for semiconductor devices, such as LSI.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In order to suppress unusual operation called field effect transistor formed in the semiconductor layer on an insulator, i.e., the substrate suspension effect which happens in SOI-MOSFET, some field-effect-transistor structures are proposed. The substrate suspension effect is good in changing the potential of a SOI layer and unusual operation occurring, when an electron hole is accumulated in the semiconductor (SOI;Silicon on insulator) layer on an insulator. In order to prevent this, it is necessary to devise the method of eliminating the l ctron hole in a SOI layer.

[0003] The n channel electric field effect type transistor shown in drawing 24 and drawing 25 is IEEE, transactions, OBU, electron DEBAISHIZU, 31 volumes, No. 8, and 1391 pages (IEEE Trans.Electron Devices, Vol.35, No.8, p.1391) by Omura. It is describing. Drawing 24 is a plan and drawing 25 is a cross section here.

[0004] The gate electrode 102 is formed through a gate insulator layer on a semiconductor layer, and the source 101 and the drain 103 are formed on both sides of the gate electrode 102. The drain field 103 is n+ which introduced n type impurity into high concentration. n+ which consisted of a field and introduced n type impurity into the source field 101 at high concentration A field 104 and p+ which introduced p type impurity into high concentration The field 105 is formed. The semiconductor layer (SOI layer 108) is formed on the embedding oxide film 109.

[0005] The electron hole generated in the channel formation field under the gate electrode 102 goes via the semiconductor layer located under the gate electrode 102, and is p+. It flows to the field contiguous to a field 105, and is eliminated through p type field 105 after that. For this, an electron hole is n+. It is [a possible thing and] p+ to flow the semiconductor layer of the gate lower part in the direction of channel width (direction parallel to the boundary of the gate, and the source / drain field), although it cannot flow into a field. It uses, respectively that it can flow into a field easily. By eliminating an electron hole in this way, this transistor has suppressed the substrate suspension effect.

[0006] The n channel electric field effect type transistor shown in drawing 26 is describing a open patent official report and common [No. 221314 / seven to]. n+ It is p+ to the semiconductor layer which adjoins the gate electrode 102 in the source 101 which consists of a field, and the position distant from the drain 103. The field 105 is formed. This transistor has the feature of being symmetrical with the source/the direction of a drain, centering on a gate electrode.

[0007] Moreover, structure like drawing 30 is carried on an AII dee em, technical one, a digest, and 337 pages by fur PUREGU in 1992. At this structure, the upper part of the source field 102 is n+. A type field (104) and the lower part are constituted by p type field (105), and the aluminum wiring 111 is n+. It is in contact with the both sides of a type field and p type field. n+ of the source field upper part A type field acts as an electronic source of supply as well as the usual source. p+ of the source field lower part A field 105 is p+ in drawing 24 . An electron hole as well as a field 105 is made to flow, and it has the operation which eliminates this from a channel formation field. p+ It is eliminated through wiring or the electron hole which flowed into the type field is n+. It is eliminated by the reunion of the tunneling to a field, and an electron.

[0008] It is p+ under the source similarly. The structure of preparing a field is indicated by a open patent official report, common [No. 159767 / two to], and common / No. 94471 / three to].

[0009] At drawing 24 and 25 or 30 structures, it is p+. A field is n+. It connects mutually with a field and wiring. Moreover, when wiring is not formed, since it flows with the tunnel between bands, between high-concentration n type layer and high-concentration p type layer, it will connect electrically.

[0010] Moreover, like drawing 27 and 28, the semiconductor layer of an isolation region (field which is not an element field) is not removed, but the method of instead preparing a field screening electrode (FS gate 122) in the upper part of the semiconductor layer of an isolation region is indicated by Iwamatsu and others at the JP,7-94754,A official report.

[0011] It is a cross section [in / A104-A104' / drawing 27 and / in drawing 28] here. / a plan

[0012] In this case, an electron hole passes along the lower part of the FS gate 122, and is eliminated through the body contact 133.

[0013] Moreover, structur like drawing 29 is indicated by a open pat nt official r port and common [5-114734]. This is n+ on the SOI layer 108. While preparing the source / drain field which consists of contest 145 polysilicon, it is p+ to the opposit side of th gate electrode 102, in view of the sourc 101. A field 105 and contest 146 p polysilicon ar formed. The electron hole generated in the channel field pass s along th lower part of th source / drain field, and is p+. It is eliminated from a field 105 and contest 146 p+ polysilicon.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] The electron hole generated in the channel section in the structure of the electric-field type transistor of this invention is p+ formed in the extended field 27 through the low concentration field 26 and the low high-impurity-concentration band 21 of the source / drain field lower part. It flows into a field 8 and can eliminate through the body contact 9. Therefore, the electron hole leading to the substrate suspension effect is eliminated.

[0115] p+ Since it is isolated by the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension, there is no mutual flow of a field 8, and five the source / drain field. That is, it also sets not only to the source but to a drain field, and is p+. The leakage current does not flow with the tunnel between bands etc. between fields. Therefore, body contact can be symmetrically prepared in the source / drain field of both sides.

[0116] Moreover, since it is not necessary to prepare the semiconductor layer used as the path of an electron hole in the bottom of the gate, the parasitic capacitance between a gate electrode and its semiconductor layer is not attached. Moreover, since body contact is prepared in the portion which extended the source / drain field in the direction of channel width, it is applicable also to the structure which transistors, such as a gate array, connected continuously.

[0117] Moreover, it is p+ by the body plug. It is p+ when a field and the silicon substrate [directly under] of it are connected. It is not necessary to make the wiring which connects a field and a grounding conductor. Furthermore, it is p+. It embeds at the silicon substrate 10 connected with a field, and is p+. If a field is prepared, a flow of the lectron hole in a silicon substrate can be improved.

[0118] Moreover, with the structure of passing an electron hole, the low high-impurity-concentration band 21 is not formed, but the field which introduced the impurity into the portion which touches the source / drain field among the extended fields 7 at low concentration is established in the bottom of the source / drain field. Then, the low concentration field in an extended field is p+. It has the operation which eases the electric field between a field, and the source / drain field 5. If electric field are eased, the tunnel current between bands will decrease and the leakage current will be suppressed.

[0119] Moreover, when forming the low high-impurity-concentration band 21 in some fields of the direction of channel width, the source / drain field 5 may reach the background of the semiconductor layer 2. In this case, from the channel field under a gate electrode, after an electron hole reaches the low high-impurity-concentration band 21, it is discharged from the extended field 7. In this case, since the source / drain field may arrive at the bottom of a SOI layer, it is not necessary to form shallow junction and the usual ion implantation etc. has the merit that the existing process can be used, to formation of the source / drain field.

[0120] Moreover, it is p+ to an extension 7. While the rectifying action will protect that a surplus charge flows from the metal section even if the metal section serves as high potential if a field is not prepared, but a metal is contacted directly and Schottky contact is taken, an electron hole [surplus / in a SOI layer] can be eliminated.

[0121] Moreover, the source of each other is connected with body contact in the electrode used as the source. It sets to the field used as a drain, and is p+. It is made not to open a contact hole in the field upper part. It sets to the field which serves as a drain by this while being able to simplify wiring, and is p+. It also sets to any when not passing, when the wiring which connects the field upper part to a drain passes, and is p+. It can prevent a field and a drain electrode short-circuiting electrically.

[0122] if low-concentration n type field is established in the lower part of the source / drain field and the silicon substrate under an embedding oxide film is made into grounding potential (0V) or an electronegative potential in an n channel electric field effect type transistor — n- under the source / drain field n type with which a depletion layer is formed in a field and polarity differs from an electron hole — it is also — it does not start but an electron hole becomes easy to flow

[0123] In the first conductivity-type electric field effect type transistor, the middle insulator layer 21 is formed in the middle of a semiconductor layer and a gate electrode in the field to which the source / drain field is not adjoined, and a semiconductor layer is located in the lower part of a gate electrode. Or the concentration of the second conductivity-typ impurity of the semiconductor layer of this field is rais d. Sinc th threshold voltage in th semiconductor layer of this portion go s up, the capacity between gate-chann ls stops th n, attaching to this portion. The demerit in the working spe d by the effective width of the source / drain field decreasing by this can be reduced.

[0124] The source / drain field, and p+ The high impurity concentration located in the middle of a field covers with the wiring which connects a low field (the low high-impurity-concentration band 21 or low high-impurity-

concentration field 32 of an xtension) to the wiring or the source linked to body contact. Then, an electron hole becomes easy to flow to these fields, and exclusion of a SOI layer to an electron hole becomes easy.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] An n channel transistor is stated to an example about the technical problem of the conventional technology.
[0015] It sets in the structure by drawing 24 and the conventional technology shown in 25 and 26, and is p+. A field 105 has the first technical problem [say / that a channel is not formed effectively] in the field which touches the gate electrode 102. The charge which forms a channel in an n channel transistor is n+. It is p+ although supplied from the source of type. If a field 105 is formed, from this field, the charge which forms a channel will not be supplied but the efficiency-width of face of the source will decrease. As for this, the actual value of channel width (the length of the boundary of the source/drain, and the gate) will fall. If the actual value of channel width d creases, the current which flows a channel will decrease. p+ Since a gate capacitance (load-carrying capacity b tween the gate and a channel) is attached to the lower part of the gate electrode which adjoins P field when a field is prepared, although the gate capacitance of the part is increasing, since there is no contribution to which fficiency-channel width is made to increase, it is p+. A working speed falls compared with the case where a field is not prepared.
[0016] This technical problem passes an electron hole in the gate lower part in the direction of channel width (direction parallel to the boundary of the source / drain field, and the gate), and is p+. It leads to a field, it originates in the principle of operation of eliminating an electron hole from p type field, and generates inevitably.
[0017] Moreover, with drawing 24 and the structure of 25, 29, and 30, the structure of a transistor has the second technical problem are not symmetrical, centering on a gate electrode.
[0018] In a general electric field effect type transistor, the source / drain field can have the same structure, and can change it mutually. These conventional examples are p+ to it. The field with a field is used only as the source and cannot be used as a drain. This is p+ to the drain which becomes a high-voltage side. It is p+ when there is a field. A field is n+ used as the high voltage. Since it connects with the field and becomes a high voltage also in itself, it is P+ by the side of a drain. Also in the state where the field and n field by the side of the source became forward bias, and the OFF signal was inputted into the gate, it is for a lot of leakage current to flow.
[0019] As for the transistor used for the transfer gate, a DRAM (dynamic RAM) cell, etc., any shall become a high-voltage side between the source / drain field changes dynamically depending on circuit operation. In order to use for these purposes, the structure of a transistor is symmetrical and the source / drain field must be able to be changed according to a situation. Therefore, an unsymmetrical transistor cannot be used for the transfer gate, a DRAM cell, etc.
[0020] Moreover, by LSI, such as a gate array, the diffusion layer etc. is formed without deciding a use beforehand, and a circuit pattern is decided afterwards according to a use. Therefore, it is decided any any of the source / drain field serve as the source, and serve as a drain after a circuit pattern is decided, and it is not decided at the time of diffusion layer formation. Therefore, it is necessary to form the transistor whose source / drain field are compatibility, and the source and the unsymmetrical transistor to which the role of a drain is fixed cannot be used in a gate array.
[0021] Moreover, it is p+ in order to create unsymmetrical structure. Although it is necessary to use as a mask the resist by which patterning was carried out so that a field may be started on a gate electrode, and it is necessary to make to either the source or a drain field with an ion implantation, with a transistor with short gate length (width of face of the gate electrode in the direction which connects a drain to the source), the patterning work of such a resist becomes very difficult.
[0022] Moreover, since a SOI transistor does not have a semiconductor layer in an isolation region (field in which no sources, drains, and channels are formed), in an isolation region, a parasitic capacitance is not attached between a wiring-semiconductor layer or a gate-semiconductor layer. However, with drawing 27 and the structure of 28, since a parasitic capacitance is attached to wiring, the gate, and field SHIDORU inter-electrode by preparing a field screening electrode (FS gate), it has the third technical problem [say / that the advantage of a SOI transistor is lost]. Moreover, with this structure, in order to form a field screening electrode, it has the fourth technical problem that a proc ss becomes complicated.
[0023] With the structure of drawing 29 , since body contact (105 146) sees from the source 101 and is in th opposite side of the gate 102, as shown in drawing 31 , it has the fifth technical problem [say / that it cannot use] in a pattern to which a transistor is connected continuously. Moreov r, although the source / drain field is form d with contest polysilicon, contest polysilicon usually has the sixth technical problem that parasitism resistanc is strong, compared with the singl crystal silicon with which the source and a drain are formed.

[0024] With drawing 27 and 28 or 29 structures, it has the seventh technical problem that the circuit pattern for body contact is all needed. Although it has the featur that well contact is omitted and wiring can b simplified, in the feature of a silicon-on-insulator desubstrate, the advantage is lost with such structures.

[Translation done.]

* NOTICES *

MEANS

[Means for Solving the Problem] this invention is solved considering the technical problem which the field effect transistor of the above-mentioned conventional technology has as the purpose.
[0026] The field effect transistor of this invention prepares a gate electrode through a gate insulator layer on the semiconductor layer on an oxide film, and sets it in the semiconductor layer of the both sides of a gate electrode. Th upper part at least the source / drain field where the impurity of the first conductivity type was introduced into high concentration Nothing, The field where the field (low high-impurity-concentration band) which adjoins the source / drain field on both sides of the lower field or lower gate electrode of the source / drain field introduced the impurity into low concentration Nothing, Projected from the low field of this high impurity concentration in the direction parallel to the boundary of the gate, and the source / drain field. The extended field which consists of a semiconductor is prepared and the field which introduced the second conductivity-type impurity into high concentration in part at least in the extended field is prepared. Between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field, high impurity concentration is characterized by preparing the low field in the field contiguous to this source / drain field whose part or gate l ctrode of an extended field is pinched.
[0027] In this invention, through the low high-impurity-concentration field of the source / drain field lower part, or the low high-impurity-concentration field of the width, an electron hole reaches an extension and is eliminated from the field which introduced the second conductivity-type impurity into high concentration by the above-mentioned composition.
[0028] The first above-mentioned technical problem in the conventional technology is p+ which passed the electron hole in the direction of channel width in the gate lower part, and was prepared in contact with the channel formation field (semiconductor region of the gate electrode lower part). It leads to a type field and is p+. From a type field, it originates in the structure of eliminating an electron hole, and generates.
[0029] On the other hand, p+ which passes an electron hole in the perpendicular direction to the direction of channel width in a low high-impurity-concentration field, and adjoins a low high-impurity-concentration field in this invention The electron hole is eliminated from.the field. Since it becomes a path for the low high-impurity-concentration field of the source / drain field lower part or the low high-impurity-concentration field of the width passing an electron hole in the perpendicular direction to the direction of channel width, a channel formation field is touched, and it is p+. It is not necessary to prepare a type field. Therefore, p+ By preparing a field, the problem whose efficiency-channel width decreases can be solved or suppressed, and the first technical problem is canceled or suppressed.
[0030] An impurity does not have the field (low high-impurity-concentration band) introduced into low concentration in the field which adjoined the source / drain field on both sides of the gate electrode especially, but in a part of this extended field, when high impurity concentration prepares a low field, there is no efficiency-reduction of channel width between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field.
[0031] Moreover, it also sets, when establishing the field (low high-impurity-concentration band) which introduced the impurity into low concentration in the field which adjoined the source / drain field on both sides of the gate electrode, and it is p+. Since the width of face can be narrowed compared with the case where adjoin a gate electrode and a field is prepared, efficiency-reduction of channel width can be suppressed.
[0032] The reason is as follows. p+ When a gate electrode is adjoined and it prepares a field, it is necessary to prepare the contact field linked to wiring into it. Therefore, p+ in the conventional technology Only the width of face of contact and the width of face containing the fixed margin surrounding it are needed, and, as for a field, bigger width of face than width of face indispensable for exclusion of an electron hole is needed. In the structure of this invention, since the contact for eliminating an electron hole is taken to the extended field distant from the gate, it is not generated but this problem can make small width of face of the field which introduced the impurity contiguous to this sourc / drain fi ld into low concentration.
[0033] Moreover, sinc th low low high-impurity-concentration band of high impurity concentration and an xtension ar between the fi ld which introduced the second conductivity-typ impurity into high concentration, and the source / drain field and a depletion layer is formed in these fields, it is p+. Electric field are ased by th depletion layer betwe n a fi ld and n field, and the flow by th tunn l betwe n bands is barred. Th refore, p+ A fi ld is prevented from the potential of n fi ld being interlocked with.
[0034] Therefor , it is p+ v n if the field which introduced the second conductivity-type impurity into high

concentration is in a drain side. Since the potential of a field does not rise, the leakage current does not flow. Since the field which introduced the second conductivity-type impurity into high concentration can be established in a drain side and symmetrical structure is acquired, the second above-mentioned technical problem resulting from unsymmetrical structure is solved. Moreover, since a field screening electrode is not prepar d, the third and the fourth technical problem are solved. Moreover, since body contact sees from the source / drain field and there is in the direction of channel width, the fifth technical problem is solved.

[0035] Moreover, in the state where grounding potential is given to the source / drain field, the high impurity concentration of the second conductivity type of the source / drain field lower part is low set up so that all th lower parts of the source / drain field may become a depletion layer.

[0036] Then, under the source / drain field, a depletion layer reaches the bottom of a SOI layer. Thereby, since the parasitic capacitance of the drain field lower part decreases, a working speed improves. Moreover, since the potential of a depletion layer is lower than the source / drain field, the depletion layer of the source field lower part can make it become the path of an electron hole, although an electron hole flows the low place of potential.

[0037] Moreover, when the voltage used as the threshold in which a channel is formed is applied to a gate electrode, the high impurity concentration of a semiconductor layer is set up so that all the semiconductor layers located in the gate electrode lower part may turn into a depletion layer. If all become [the semiconductor layer located in the gate electrode lower part] a depletion layer, it will be hard coming to accumulate an electron hole (if a perfect depletion is formed). This reduces the burden about the exclusion capacity of an electron hole, and is a book.

[0038] this invention touches a gate electrode and is p+. A field is not prepared, but it lets the low field of high impurity concentration pass, and is an electron hole p+ It leads to a field. The low field of high impurity concentration is p+. Although the capacity to pass an electron hole compared with a field is inferior, the problem that the capacity to pass an electron hole is inferior can be offset by reducing accumulation of an electron hole by perfect depletion-ization.

[0039] Moreover, it does not have the field which introduced the impurity into low concentration in the field which adjoined the source / drain field on both sides of the gate electrode, but high impurity concentration prepares a low field in a part of this extended field between the field which introduced this second conductivity-type impurity into high concentration, and the source / drain field.

[0040] Also in this case, since an electron hole can be discharged via the bottom of the source/drain, the second above-mentioned technical problem is solvable.

[0041] Moreover, the second conductivity-type impurity prepared in a part of extended field is connectable with the semiconductor layer or conductor layer under an oxide film. It is not necessary to prepare the body contact which met with wiring in contact with the transistor, and the seventh above-mentioned technical problem can be solved.

[0042] Moreover, the source / drain field is formed from an epitaxial layer, a low concentration field is established in the bottom of it, and if a low concentration field is connected to the high high-impurity-concentration field of the second conductivity type in the field distant from the source / drain field, since the source/drain will become a single crystal, the sixth above-mentioned technical problem is solved.

[0043] Moreover, the second conductivity-type field of high high impurity concentration is not established in an extended field, but a metal is directly contacted to an extension.

[0044] Moreover, the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode is adjoined, and an insulator layer thicker than the gate insulator layer of other fields is prepared between a gate electrode and the semiconductor layer located in the bottom of it in the field located in the gate electrode lower part at a semiconductor layer. Or the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode is adjoined, and concentration of the second conductivity-type impurity is made higher than other fields under a gate electrode in the semiconductor layer located in the gate electrode lower part.

[0045] By these, the semiconductor layer in which the source/drain is not formed on both sides of a gate electrode is adjoined, threshold voltage of the field located in the gate electrode lower part at a semiconductor layer is made high, and formation of a channel can be suppressed. A channel becomes the low high-impurity-concentration band 21 is hard to be formed, and the capacity between gate-channels stops then, attaching to this portion. The problem relevant to the first above-mentioned technical problem that the effective width of the source / drain field decreases by this, without the capacity between gate-channels becoming less is mitigated.

[0046] Moreover, it is made for the wiring which is formed in the field contiguous to this source / drain field whose part or gate electrode of this extended field is pinched and which high impurity concentration connected to the source on the insulator layer on a low field to be located.

[0047] Or it is made for the wiring which connected this second conductivity-type impurity to the upper part of these fields to the field introduced into high concentration to be located.

[0048] If these fields are covered by the wiring which connected the wiring or this second conductivity-type impurity linked to the source to the field introduced into high concentration, these low high-impurity-concentration fields will become lower than grounding potential (or potential of wiring). Since an electron hole flows the low place of potential, an electron hole becom s easy to flow to th se fields.

[0049]

[Embodiments of the Invention] H reafter, the form of operation of this inv ntion is described, referring to a drawing.

[0050] The plan of the field ffect transistor based on this invention is shown in drawing 1 about th case of an n channel transistor. A1-A1'cross-section and B1-B1' the cross s ction of drawing 1 is shown in drawing 2 and

drawing 3 , respectively.
[0051] The gate electrode 4 is formed on the semiconductor layer 2 on an oxide film 11. Setting in the semiconductor layer 2 whose gate electrode 4 is pinched, the upper part is n+. It is p which diffused the impurity of concentration with the low lower part of nothing and the semiconductor layer 2 for the type source drain field 5. - A field 26 is made. The gate insulator layer 3 is formed in the lower part of the gate electrod 4, and the s miconductor layer 2 of the lower part of a gate electrode mak s the channel formation field 27. It connects with the wiring which the source / drain contact 23 is form d on th source / drain field 5, and consists of aluminum 24. in order [however,] to make element structure intelligible — aluminum 24 — the drawing 3 **** — only — it is shown
[0052] The low high-impurity-concentration band 21 of the semiconductor layer 2 with which the source / drain field 5 was established in neither in a semiconductor layer and on a layer in the field, but the impurity was introduced into low concentration is made in part. The extended field 7 which furthermore projected from the low high-impurity-concentration band 21 in the direction of channel width is formed. However, a direction parallel to the source / drain field, and the boundary of a gate electrode is called direction of channel width here. p+ which introduced p type impurity into a part of extended field [at least] 7 at high concentration A field 8 is formed, the body contact 9 is formed in p field, and it connects with the wiring which consists of aluminum 24. The wiring connected to the body contact 9 maintains grounding potential, or if it is potential [at least] smaller than the band gap of a semiconductor layer, for example, silicon, it will maintain the potential not more than 1.12V. The potential of the wiring connected to body contact is grounded, or when it is negative, the electron hole exclusion capacity of body contact becomes high. However, a certain amount of exclusion capacity is acquired as potential is higher than grounding potential. However, if it becomes higher than the potential equivalent to a band gap, since the leakage current from body contact to the source will become remarkable, this needs to avoid.
[0053] The electron hole generated in the channel section in this structure is p+ formed in the extended field 7 through the low concentration field 26 and the low high-impurity-concentration band 21 of the source / drain field lower part. It flows into a field 8 and can eliminate through the body contact 9. Therefore, the electron hole leading to the substrate suspension effect will be eliminated.
[0054] The first technical problem (fall of efficiency-channel width) in the conventional technology passes an electron hole in the direction of channel width in the gate lower part, and is p+. p+ which led to the field and was prepared in contact with the channel formation field (semiconductor region of the gate electrode lower part) From a type field, it originates in the structure of eliminating an electron hole, and generates.
[0055] On the other hand, p+ which passes an electron hole in the perpendicular direction to the direction of channel width in a low high-impurity-concentration field (21 26), and adjoins a low high-impurity-concentration field in this invention An electron hole is eliminated from a field 8. Since it becomes a path for the low high-impurity-concentration field 26 of the source / drain field lower part or the low high-impurity-concentration field 21 of the width passing an electron hole in the perpendicular direction to the direction of channel width, a channel formation field is touched, and it is p+. It is not necessary to prepare a type field. Therefore, p+ By preparing a field, the problem that efficiency-channel width falls can be solved or suppressed, and the first above-mentioned technical problem is solved.
[0056] It does not have the low high-impurity-concentration band 21 especially, but they are the source / drain field, and p+. The low concentration field 32 is formed between fields, and there is no efficiency-reduction of channel width with the structure (drawing 13 and its B13-B13' cross section, drawing 14) which has the low concentration field 26 under the source / drain field. Moreover, it also sets, when forming the low high-impurity-concentration band 21, and it is p+. Since width of face of the low high-impurity-concentration band 21 can be narrowed compared with the case where adjoin a gate electrode and a field is prepared, efficiency-reduction of channel width can be suppressed.
[0057] The reason is as follows. It is p+ like the conventional example (25 drawing 24 , 26). When a gate electrode is adjoined and it forms a field 105, it is necessary to prepare the contact field linked to wiring into it. Therefore, p+ in the conventional technology Only the width of face of contact and the width of face containing the fixed margin surrounding it are needed, and, as for a field, bigger width of face than width of face indispensable for exclusion of an electron hole is needed. In the structure of this invention, since the contact for eliminating an electron hole is taken to the extended field 7 distant from the gate, width of face of the low high-impurity-concentration band 21 can be made small, and the first above-mentioned technical problem can be suppressed.
[0058] p+ Since it is isolated by the low high-impurity-concentration band 21 or the p field 32, there is no mutual flow of a field 8, and five the source / drain field. That is, the field strength between both is eased by isolating both (p+ field, and the source/drain). Therefore, when a drain becomes high potential, it can prevent strong electric field's becoming a cause and the tunnel current between bands flowing among both. Therefore, p+ Even if a field is in a drain side, a drain and the leakage current during body contact do not flow. Therefore, body contact can be prepared in both the source / drain field, and the second above-mentioned technical problem (asymmetry) can be solved.
[0059] Mor over, it is p+ like drawing 24 and the conventional example of 26. A field is touched, and since it is not necessary to prepar the semiconductor layer located und r th gate as a path of an lectron hol , the parasitic capacitance b tween a gate electrod and its semiconductor layer is not attached. Moreover, sinc a field screening electrode like the conventional example of drawing 27 is not prepared, the above-mention d third and the fourth technical problem are solvable.
[0060] Moreover, since body contact is prepared in th portion extended in the direction of channel width from the

source / drain field, it is applicable also to the connected structure in which the gate array etc. carried out transistor continuation. Therefore, the fifth above-mentioned technical problem is solved.
[0061] Hereafter, the form of other operations is described.
[0062] In the state where grounding potential is given to the source / drain field, the high impurity concentration of the second conductivity type of the source / drain field lower part can be low set up so that all th lower parts of the first conductivity-typ source / drain field may become a depletion layer.
[0063] Then, und r th source / drain field, a depletion layer reaches th bottom of a SOI layer. Thereby, sinc the parasitic capacitance of the drain field lower part decreases, a working speed improves. Moreover, although an electron hole flows the low place of potential, since the potential of a depletion layer is lower than the source / drain field, the depletion layer of the source field lower part is made as for a bird clapper to the path of an electron hole.
[0064] Moreover, when the voltage used as the threshold in which a channel is formed is applied to a gate electrode, th high impurity concentration of a semiconductor layer can be set up so that all the semiconductor layers located in the gate electrode lower part may turn into a depletion layer. ** for which an electron hole stops being able to accumulate easily since the potential of the field will go up, if all become [the semiconductor layer located in the gate electrode lower part] a depletion layer. This reduces the burden about the exclusion capacity of an electron hole, and is a book.
[0065] this invention touches a gate electrode and is p+. A field is not prepared, but it lets the low field of high impurity concentration pass, and is an electron hole p+ It leads to a field. The low field of high impurity concentration is p+. Although the capacity to pass an electron hole compared with a field is inferior, the problem that the capacity to pass an electron hole is inferior can be offset by reducing accumulation of an electron hole by perfect depletion-ization.
[0066] Moreover, drawing 4 , and 5, 6 and 7 are p+. It is explanatory drawing of the form of operation of this invention in case it does not connect with wiring 24 but a field 8 is connected with a silicon substrate 10 by the body plug 15, and, for drawing 4 and drawing 5 , the body plug 15 is p+. When piercing through a field, drawing 6 and drawing 7 are p+. It is the case where it touches from the side without piercing through a field. For drawing 8 , the body plug 15 is p+. It is the case where a field 8 is touched from the bottom.
[0067] p+ Since it connects with silicon machine 10 boards [directly under] of it and an electron hole is discharged by the silicon substrate 10, a field 8 is p+. It is not necessary to make the wiring which connects a field and a grounding conductor. Moreover, it embeds into the portion which touches the body plug 15 at a silicon substrate 10, and is p+. The case where a field 28 is formed is shown in drawing 9 and drawing 10 . It embeds at a silicon substrate 10 and is p+. If a field is prepared, a flow of the electron hole in a silicon substrate will be improved.
[0068] The case where the source / drain field is formed by the epitaxial layer 30 in the structure of drawing 1 is shown in drawing 11 . By diffusing Lynn from an epitaxial layer shallowly, it is n+ to the front face of a semiconductor layer. A field 31 is formed shallowly.
[0069] In drawing 1 , the case where the low high-impurity-concentration band 21 is not formed is shown in drawing 13 and drawing 14 . In this case, it is p to the portion which touches the source / drain field among the extended fields 7. - A field 32 is formed. In this case, p in the extended field 7 - A field 32 replaces the low high-impurity-concentration band 21, and is p+. It has the operation which eases the electric field between a field, and the source / drain field 5. Moreover, p in the low high-impurity-concentration band 21 and the extended field 7 - You may form both fields 32.
[0070] Moreover, the cross section in B1-B1' in case the source / drain field 5 reaches the background of the semiconductor layer 2 is shown in drawing 15 by the case where the low high-impurity-concentration band 21 is formed. In this case, after an electron hole flows the channel field under a gate electrode in the direction of channel width and reaches the low high-impurity-concentration band 21, it is discharged from the extended field 7. In this case, since the source / drain field may arrive at the bottom of a SOI layer, it is not necessary to formation of the source / drain field to form shallow junction.
[0071] Moreover, it sets in the structure of drawing 13 and is p+ to an extension. A field is not prepared, but a metal is contacted directly and the case where Schottky contact (connection of wiring 24 and the low concentration layer 21) is taken is shown in drawing 17 . In this case, you may use a tungsten, tungsten silicide, etc. for wiring. Moreover, in order to adjust the size of the Schottky barrier, you may also insert metals, such as TiN and tungsten silicide, or the compound containing a metallic element as an interlayer between the low concentration layer 21 and wiring 24. In this case, Schottky contact is formed of the low concentration layer 21 and an interlayer.
[0072] The Schottky contact in which the metal was contacted has a rectifying action in a low-concentration semiconductor layer. The band view in the case (in the low case [The potential by the side of a metal]) of grounding the metal which forms Schottky contact is shown in drawing 32 . Although a surplus electron hole can flow to a metal side, an electron cannot flow because of the obstruction formed in the semiconductor layer (p-field) of low concentration [side / channel / side / metal]. Moreover, the case where the potential by the side of a metal is high is shown in drawing 33 and drawing 34 . If a metal is contacted to high p substrate of p type high impurity concentration, since it will b com lik drawing 33 , a thin obstruction will be formed in the field in which a d pl tion layer is formed in p substrate in contact with a metal and an el ctron hole will pass through this obstruction according to a tunnel phenomenon, an excessive hole current will be poured in from a metal sid . On the other hand, a metal is low-conc ntration p like this invention. - The case where a field or th intrinsic (i) field is contacted is shown in drawing 34 . In this cas , sinc a low concentration field and i field are influenced of drain voltage and

become the voltage near drain potential, the obstruction over an electron hole is formed like drawing 34 , and an electron hole is not poured in. Since the field influenced of drain electric field serves as an obstruction as shown in drawing 34 when a low concentration field connects this to a channel through the low concentration field under a drain like especially drawing 13 , it is remarkable ineffective.

[0073] Mor over, drawing 18 shows the state where the structure of drawing 1 was connected when two or more transistors, such as a gat array, were connected and had been arrang d, and drawing 19 is p+. A field 8 is extended and the example which formed the body contact 9 outside the contact 22 to a gate electrod is shown. Lik drawing 18 , body contact is p+. You may open so that a field may be covered. (The margin of p+ field which surrounds contact is not taken) .

[0074] Moreover, in a gate array, the source of each other is connected with body contact in the electrode used as the source. It sets to the field used as a drain, and is p+. It is made not to open a contact hole in the field upper part. This sets to the field used as a drain, and it is p+. It also sets to any when not passing, when the wiring which connects the field upper part to a drain passes, and is p+. It can prevent a field and a drain electrode short-circuiting electrically.

[0075] When it is not decided like the transfer gate any shall be on a high-voltage side between the source / drain field, body contact is not connected with the source / drain field, but all body contacts are grounded. That is, it connects with wiring with grounding potential.

[0076] Moreover, the low concentration field of the source / drain field lower part is n to drawing 20 . - The case where it is type is shown.

[0077] p- When a silicon substrate is grounded, it is p from the relation of a work function. - A substrate serves as potential lower than the source. Moreover, even if it gives an electronegative potential to a silicon substrate, a silicon substrate serves as potential lower than the source similarly. Then, even if it establishes n-field in the bottom of the source / drain field, a depletion layer is formed in this field of the influence of the electric field from a substrate. if a depletion layer is formed — n- n type with which polarity differs from an electron hole since the potential of a field 40 falls — it is also — it does not start but an electron hole becomes easy to flow

[0078] Drawing 21 shows the case where the oxide film on the field (channel field contiguous to a low high-impurity-concentration band) inserted into the low high-impurity-concentration band 21 is made thicker than a gate oxide film (the middle insulator layer 41 of drawing 21 and drawing 21 are equivalent to the D1-D1' cross section of drawing 1). If the middle insulator layer 41 is formed, the threshold voltage of this portion will go up. If this has a thick gate oxide film, it will be based on the principle that threshold voltage goes up. A channel becomes is hard to b formed in the field contiguous to the low high-impurity-concentration band 21, and the capacity between gate channels (gate capacitance) stops then, attaching to this portion.

[0079] Thereby, the influence of the effective width of the source / drain field decreasing can be reduced by forming the low high-impurity-concentration band 21. Although it is disadvantageous, if the effective width of the source / drain field decreases without the capacity between gate-channels becoming less, and the capacity between gate-channels becomes less with the effective width of the source / drain field to a working speed, the demerit over a working speed can be reduced.

[0080] Moreover, the middle insulator layer 41 may cover the low high-impurity-concentration band 21 top. In this case, the effect that the capacitive component between a low high-impurity-concentration band and the wiring arranged on it is mitigable is acquired.

[0081] Moreover, if p type high-impurity-concentration band of a low high-impurity-concentration band is increased, since the threshold voltage of this portion will go up and a channel will no longer be formed, the source / drain field can mitigate the problem that capacity is attached in the portion (portion pinched by the low high-impurity-concentration band 21) which does not work effectively, also by this method.

[0082] Moreover, the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension can be covered with the wiring 42 linked to body contact. If p type impurity is introduced into the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension, potential will become low rather than the wiring which these fields have in the upper part. If grounding potential has body contact, these low high-impurity-concentration fields (21 32) will become lower than grounding potential. Since an electron hole flows the low place of potential, an electron hole becomes easy to flow to these fields (21 32).

[0083] Moreover, the example which covered the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension with the wiring 43 linked to the source / drain field in the structure of drawing 13 is shown in drawing 23 . As for a source side, although either the source or a drain field operate as the source, since potential is low, like the case where it covers by the result above-mentioned grounding conductor, an electron hole becomes easy to flow to a low high-impurity-concentration field by the source side, and an electron hole becomes is easy to be eliminated.

[Translation done.]

EXAMPLE

[Example]
The plan of the field effect transistor based on this example is shown in example 1 drawing 1 . A1-A1'cross-section and B1-B1' the cross section of drawing 1 is shown in drawing 2 and drawing 3 , respectively.
[0085] It is n+ so that the semiconductor layer 2 may be crossed on the semiconductor layer 2 on an oxide film 11. The gate electrode 4 with a width of face of 0.25 microns which consists of contest polysilicon is formed. The gate insulator layer 3 with a thickness of 5nm is formed in the lower part of the gate electrode 4. It is p to which the lower part of nothing and the semiconductor layer 2 diffused the p type impurity for the source drain field 5 where the upper part diffused the n type impurity in high concentration to low concentration in the semiconductor layer 2 whose gate electrode 4 is pinched. - A field 26 is made. The semiconductor layer 2 of the lower part of a gate electrode makes the channel formation field 27 in which a channel is formed. It connects with the wiring which the source / drain contact 23 is formed on the source / drain field 5, and consists of aluminum 24.
[0086] The source / drain field 5 is not formed, but a part of semiconductor layer 2 is p. - The low high-impurity-concentration band 21 of type is made. The extended field 7 which furthermore projected from the low high-impurity-concentration band 21 in the direction of channel width is formed. However, a direction parallel to the source / drain field, and the boundary of a gate electrode is called direction of channel width here. p+ which introduced p type impurity into a part of extended field [at least] 7 at high concentration A field 8 is formed and it is p+. The body contact 9 is formed in a field and it connects with the wiring which consists of aluminum 24. The wiring connected to the body contact 9 maintains grounding potential, or if it is potential [at least] smaller than the band gap of a semiconductor layer, for example, silicon, it will maintain the potential not more than 1.12V.
[0087] In the cross section of drawing 2 and drawing 3 , in 10, a silicon substrate and 11 show an embedding oxide film, and 25 shows a layer insulation film. Thickness of an embedding oxide film and a layer insulation film was set to 400nm, respectively. Width of face [as opposed to the direction of channel width of 1 micron, and the source / drain field in width of face / as opposed to the direction of channel width of 20nm and the low high-impurity-concentration band 21 in the thickness of 60nm, and the source / drain field 5] made SOI layer thickness 10 microns. Width of face of a direction parallel to the direction of A1-A1' of an extended field was made into 0.3 microns. p- For boron, in a field 26, boron is 1x1017cm-3 and p+ to 1x1017cm-3 and the low high-impurity-concentration band 21. Boron was introduced into the field 8 and Lynn was introduced into 1x1019cm-3, and the source / drain field 1x1019cm-3. A silicon substrate is p containing the boron of concentration 1x1016cm-3. - It considered as type.
[0088] The electron hole generated in the channel section in this structure is p+ formed in the extended field 7 through the low concentration field 26 and the low high-impurity-concentration band 21 of the source / drain field lower part. It flows into a field 8 and can eliminate through the body contact 9. Therefore, the electron hole leading to the substrate suspension effect will be eliminated.
[0089] p+ Since it is isolated with the low high-impurity-concentration band 21, there is no mutual flow of a field 8, and five the source / drain field. That is, it also sets not only to the source but to a drain field, and is p+. The leakage current does not flow with the tunnel between bands etc. between fields. Therefore, body contact can be symmetrically prepared in both the source / drain field. Moreover, there is no reduction of the effective channel width accompanying formation of body contact. Moreover, since the source / drain field prepares body contact in the portion extended in the direction of channel width, it is applicable also to the structure which transistors, such as a gate array, connected continuously.
[0090] It sets to drawing 1 and example 2 this example is p+. It is the case where do not connect with wiring but the field 8 is connected with the silicon substrate 10.
[0091] For drawing 4 and drawing 6 , this example is p+, respectively. The plan and drawing 5 which expanded the field 8 neighborhood, and drawing 7 are C4-C4' in drawing 4 and drawing 6 , and an elevation in a C6-C6' cross section, respectively. It also sets to any and is p+. A field 8 is p+. It is p by the body plug 15 which consists of contest polysilicon. - It connects with the silicon substrate 10. Drawing 4 and drawing 5 are p+. When piercing through a fi ld, drawing 6 and drawing 7 are p+. It is the case wher it touches from the sid without piercing through a fi ld. For drawing 8 , a body plug is p+. It is the case where it touches from und r a fi ld. p+ Since a field is connected to the silicon substrat [directly under] of it and an el ctron hole flows into a silicon substrate, it is p+. It is not necessary to make the wiring which connects a field and a grounding conductor.
[0092] Moreover, it embeds into the portion which touches th body plug 15 at a silicon substrate 10 as shown in drawing 9 and drawing 10 , and is p+. You may form a field 28. p+ A field 28 is second p+ which pierces through an

embedding oxide film in the position distant from the transistor. It connects with a grounding conductor with the wiring which consists of a polysilicon contest plug 29 and aluminum 24 (drawing 9). Moreover, you may use a metal like aluminum 24 as a material of a plug (drawing 10). It embeds at a silicon substrate 10 and is p+. When the field was prepared, the flow of the electron hole in a silicon substrate was abl to be improved. Th body plug 15 is formed by performing embedding by CVD of plug material (conductors, such as contest p+ polysilicon, a metal, and metal silicide) etc., and etchback by continuing RIE.

[0093] Example 3 this example shows the cross section of this example to drawing 11 about the A1-A1' cross section of drawing 1 in the structure of drawing 1 by the case where the source / drain field is formed by th epitaxial layer 30. High-concentration Lynn was introduced into the epitaxial layer 30. It is n+ to the front face of a semiconductor layer by diffusing Lynn from an epitaxial layer shallowly with heat treatment by lamp annealing or the electric furnace. The field 31 was formed shallowly. n+ The thickness of a field 31 is 20nm.

[0094] Drawing 13 shows a plan and the B13-B13' cross section of drawing 13 to drawing 14 by the case where example 4 this example does not form the low high-impurity-concentration band 21 in drawing 1 . p which introduced boron into the portion which touches the source / drain field among the extended fields 7 in this structure low concentration 1x1017cm-3 - The field 32 was formed. In this case, the p-field 32 in the extended field 7 replaces the low high-impurity-concentration band 21, and is p+. It has the operation which eases the electric field between a field, and the source / drain field 5. Moreover, p in the low high-impurity-concentration band 21 and the extended field 7 - You may form both fields 32.

[0095] When forming the example 5 low high-impurity-concentration band 21, the source / drain field 5 may reach the background of the semiconductor layer 2. this example is an example in this case, and shows the cross section in that case to drawing 15 (setting in the position equivalent to the B1-B1' cross section of drawing 1). In this case, after an electron hole passes along the channel field under a gate electrode and reaches the low high-impurity-concentration band 21, it is discharged from the extended field 7. In this case, since the source / drain field may arrive at the bottom of a SOI layer, it is not necessary to form shallow junction and there is a merit that the usual ion implantation etc. can use the existing process, to formation of the source / drain field (drawing 15).

[0096] It sets in the structure of drawing 13 and example 6 this example is p+ to an extension. A field is not prepared, but a metal is contacted directly and the B13-B13' cross section in drawing 13 is shown in drawing 17 by the case where Schottky contact is taken. Moreover, the same cross section shows the case where Schottky contact is connected with the contact on the source / drain field to drawing 16 .

[0097] The Schottky contact in which the metal was contacted has a rectifying action in a low-concentration semiconductor layer. The band view in the case (when the potential by the side of a metal is low) of grounding the metal which forms Schottky contact is shown in drawing 32 . Although a surplus electron hole can flow to a metal side, an electron cannot flow because of the obstruction formed in the semiconductor layer (p-field) of low concentration [side / channel / side / metal]. Moreover, the case where the potential by the side of a metal is high is shown in drawing 33 and drawing 34 . If a metal is contacted to high p substrate of p type high impurity concentration, since it will become like drawing 33 , a thin obstruction will be formed in the field in which a depletion layer is formed in p substrate in contact with a metal and an electron hole will pass through this obstruction according to a tunnel phenomenon, an excessive hole current will be poured in from a metal side. On the other hand, a metal is low-concentration p like this invention. - The case where a field or the intrinsic (i) field is contacted is shown in drawing 34 . In this case, since a low concentration field and i field are influenced of drain voltage and become the voltage near drain potential, the obstruction over an electron hole is formed like drawing 34 , and an electron hole is not poured in. Since the field influenced of drain electric field serves as an obstruction as shown in drawing 34 when a low concentration field connects this to a channel through the low concentration field under a drain like especially drawing 13 , it is remarkable ineffective.

[0098] Moreover, it enables this to connect the source / drain field, and body contact like drawing 16 . That is, when the source / drain field acts as the low source of potential, while an electron hole is eliminated through this, when acting as a drain with high potential, a leakage current does not occur, but symmetrical structure becomes possible.

[0099] Moreover, you may use a tungsten, tungsten silicide, etc. for wiring. Moreover, in order to adjust the size of the Schottky barrier, you may also insert metals, such as TiN and tungsten silicide, or the compound containing a metallic element as an interlayer between the low concentration layer 21 and wiring 24.

[0100] Example 7 this example is [the example (drawing 18 ; plan) which connected the structure of drawing 1 when two or more transistors, such as a gate array, were connected and it had been arranged, and] p+. It is an example (drawing 19 ; plan) in case a field 8 is extended and body contact is prepared outside the contact to a gate electrode. Body contact is p+. The source of each other is connected with body contact in the electrode from which it can open so that a field may be covered (the margin of p+ field which surrounds contact is not taken), and ** also serves as the source in a good (drawing 18) gate array. It sets to the field used as a drain, and is p+. It is made not to open a contact hole in the field upper part. This sets to the field used as a drain, and it is p+. It also sets to any when not passing, when the wiring which connects the field upper part to a drain passes, and is p+. It can prevent a field and a drain lectrode short-circuiting electrically.

[0101] When it is not decided lik the transfer gat any shall be on a high-voltage side betw en th sourc / drain field, body contact is not connect d with the source / drain field, but all body contacts ar grounded, namely, are connected to wiring with grounding potential.

[0102] For example 8 this example, the low concentration field of the source / drain field lower part is n. - By the case where it is type, the cross section is shown in drawing 20 (setting in th position equivalent to the B1-B1'

cross section of drawing 1). The lower part of the sourc / drain field is poured-in n 1x1017cm-3 about Lynn. - It considered as the field 40. A silicon substrate 10 is p. - It considered as type. It considered as grounding potential (0V) or the electronegative potential at the silicon substrate 10.
[0103] p- When a silicon substrate is grounded, it is p from the relation of a work function. - A substrat serves as potential lower than the source. Moreover, p - It is p when an electronegative potential is given to a silicon substrate. - It becomes low potential. Then, it is n under the source / drain field. - Even if it prepares a field, a depletion layer is formed in this field in response to the influence of th potential of a silicon substrate. if a d pletion layer is formed — n- n type with which polarity differs from an electron hole since the potential of a field falls — it is also — it does not start but an electron hole becomes easy to flow
[0104] Example 9 this example is an example at the time of making the oxide film on the channel formation field contiguous to the low high-impurity-concentration band 21 thicker than a gate oxide film.
[0105] In drawing 1 , the D1-D1' cross section at the time of forming the middle insulator layer 41 on the channel formation field (field under a gate electrode) which adjoins the low high-impurity-concentration band 21 and it is shown in drawing 21 .
[0106] If the middle insulator layer 41 is formed, the threshold voltage of this portion will go up. If this has a thick gate oxide film, it will be based on the principle that threshold voltage goes up. A channel becomes the low high-impurity-concentration band 21 is hard to be formed, and the capacity between gate-channels stops then, attaching to this portion.
[0107] Thereby, the influence of the effective width of the source / drain field decreasing can be reduced by forming the low high-impurity-concentration band 21. Although it is disadvantageous, if the effective width of the source / drain field decreases without the capacity between gate-channels becoming less, and the capacity between gate-channels becomes less with the effective width of the source / drain field to a working speed, the demerit over a working speed can be reduced.
[0108] Moreover, if p type high impurity concentration of a low high-impurity-concentration band is increased, since the threshold voltage of this portion will go up and a channel will no longer be formed, the source / drain field can mitigate the gate capacitance to the portion which does not work effectively also by this method.
[0109] In example 10 this example, the example which covered the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension with the wiring 42 linked to body contact in the structure of drawing 1 is shown in drawing 22 (plan).
[0110] If p type impurity is introduced into the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension, potential will become low rather than the wiring which these fields have in the upper part. If grounding potential has body contact, these low high-impurity-concentration fields will become lower than grounding potential. Since an electron hole flows time with the low of potential, an electron hole becomes easy to flow to these fields.
[0111] Moreover, the example which covered the low high-impurity-concentration band 21 or the low high-impurity-concentration field 32 of an extension with the wiring 43 linked to the source / drain field in the structure of drawing 13 is shown in drawing 23 (plan).
[0112] As for a source side, although either the source or a drain field operate as the source, potential is a low, as a result, like the upper case, an electron hole becomes easy to flow to a low high-impurity-concentration field (21 32) by the source side, and an electron hole becomes is easy to be eliminated.
[0113] As mentioned above, although the example about an n channel transistor was shown, in the case of a p-channel transistor, all polarity should just be made into reverse in the above example.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The ** type plan showing the example of this invention
[Drawing 2] The A1-A1' cross section of drawing 1
[Drawing 3] The B1-B1' cross section of drawing 1
[Drawing 4] The ** type flat-surface partial diagrammatic view of another example of this invention
[Drawing 5] The C4-C4' cross section of drawing 4
[Drawing 6] The ** type flat-surface partial diagrammatic view of another example of this invention
[Drawing 7] The C6-C6' cross section of drawing 6
[Drawing 8] The type section partial diagrammatic view of another example of this invention
[Drawing 9] The type section view of another example of this invention
[Drawing 10] The type section view of another example of this invention
[Drawing 11] The type section view of another example of this invention
[Drawing 12] The type section view of another example of this invention
[Drawing 13] The ** type plan of another example of this invention
[Drawing 14] The B13-B13' cross section of drawing 13
[Drawing 15] The type section view of another example of this invention
[Drawing 16] The type section view of another example of this invention
[Drawing 17] The type section view of another example of this invention
[Drawing 18] The ** type plan of an example with which two or more transistors of this invention are connected
[Drawing 19] The ** type plan of another example with which two or more transistors of this invention are connected
[Drawing 20] The type section view of another example of this invention
[Drawing 21] The type section view of another example of this invention
[Drawing 22] The ** type plan of another example of this invention
[Drawing 23] The ** type plan of another example of this invention
[Drawing 24] The ** type plan showing the conventional technology
[Drawing 25] The type section view showing the conventional technology
[Drawing 26] The ** type plan showing the conventional technology
[Drawing 27] The ** type plan showing the conventional technology
[Drawing 28] The type section view showing the conventional technology
[Drawing 29] The type section view showing the conventional technology
[Drawing 30] The type section view showing the conventional technology
[Drawing 31] The ** type plan explaining the trouble of the conventional technology
[Drawing 32] Book
[Drawing 33] The band view explaining the trouble of the conventional technology
[Drawing 34] Book
[Description of Notations]
1 Oxide Film
2 Semiconductor Layer
3 Gate Insulator Layer
4 Gate Electrode
5 Source Drain Field
7 Extended Field
8 P+ Field
9 Body Contact
10 Silicon Substrate
11 Embedding Oxide Film
15 Body Plug
21 Low High-Impurity-Concentration Band
23 Source / Drain Contact
24 Aluminum
25 Layer Insulation Film

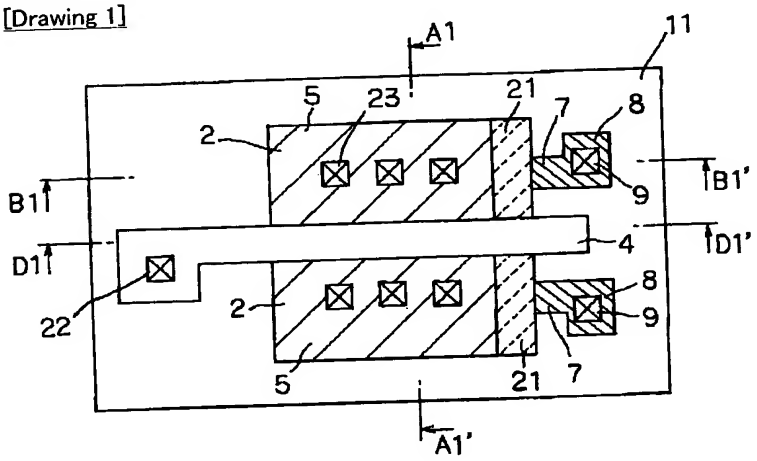
26 P - Field
27 Channel Formation Field
28 Embedding P+ Field
29 Second P+ Polysilicon Contest Plug
30 Epitaxial Layer
31 N+ Field
32 P - Field
41 Middle Insulator Layer
42 Wiring Linked to Body Contact
43 Wiring Linked to Source / Drain Field
101 Source
102 Gate
103 Drain
104 N+ Field
105 P+ Field
106 Gate Oxide Film
107 P Field
108 SOI Layer or P - Field
109 Embedding Oxidizing Zone
110 Silicon Substrate
111 Aluminum Wiring
112 Oxide Film
120 P+ Field
121 P Field
122 FS Gate
123 FS Gate Oxide Film
124 Gate Oxide Film
125 Gate Electrode
126 First Oxide Film
127 Second Oxide Film
130 Source / Drain Field
131 Gate Contact
132 FS Gate Contact
133 Body Contact
134 P++ Field
141 Drain Electrode
142 Source Electrode
143 Wiring Electrode
144 Contact
145 N+ Contest Polysilicon
146 P+ Contest Polysilicon

[Translation done.]

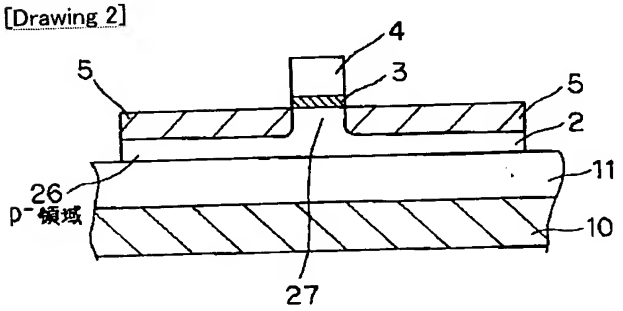
* NOTICES *

DRAWINGS

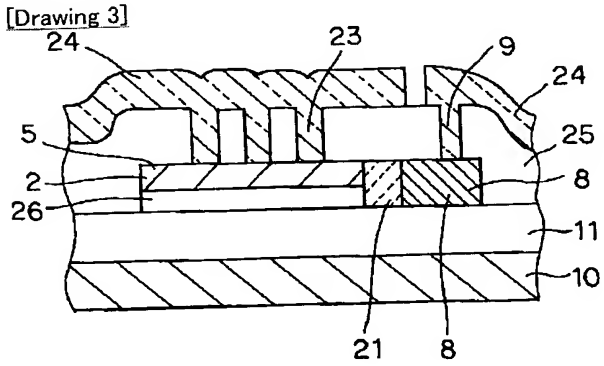
[Drawing 1]



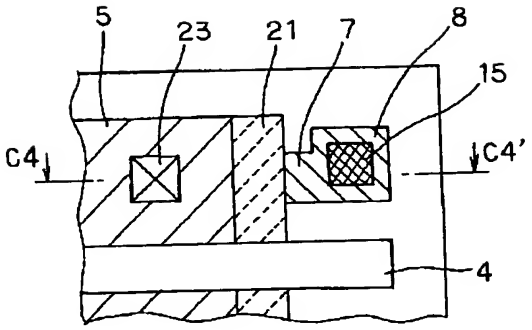
[Drawing 2]



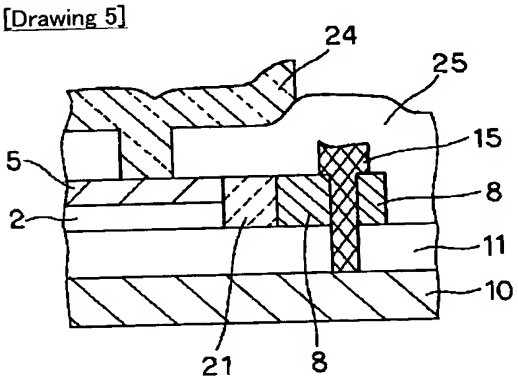
[Drawing 3]



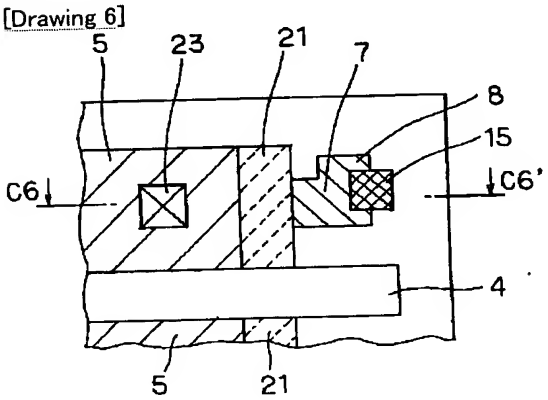
[Drawing 4]



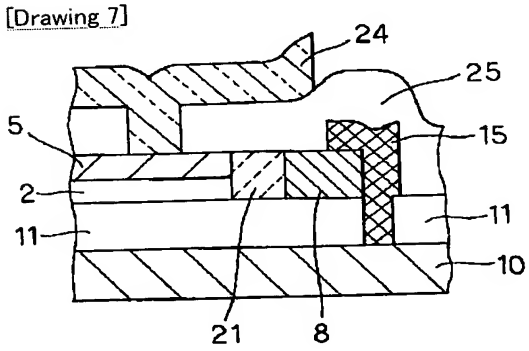
[Drawing 5]



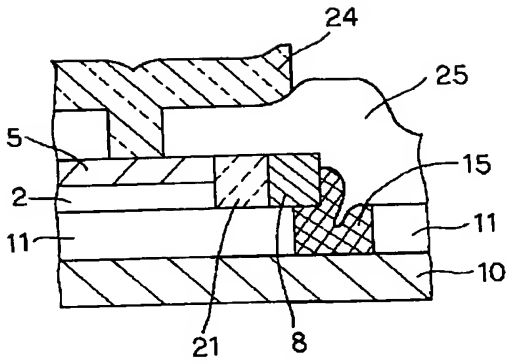
[Drawing 6]



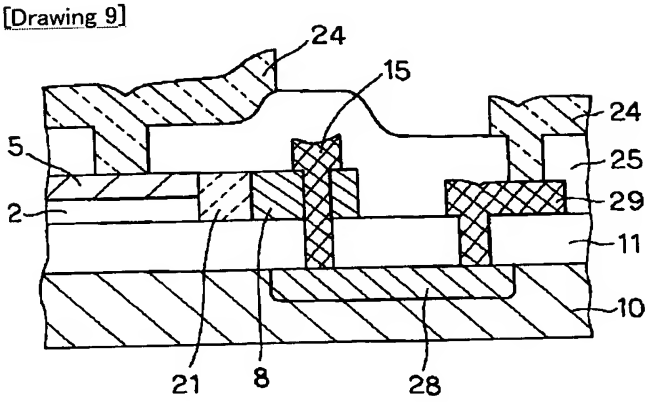
[Drawing 7]



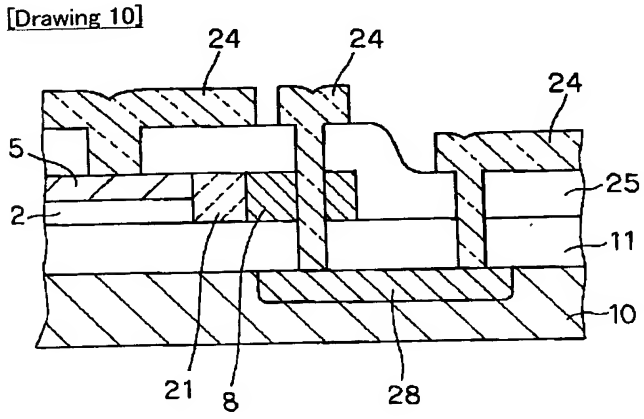
[Drawing 8]



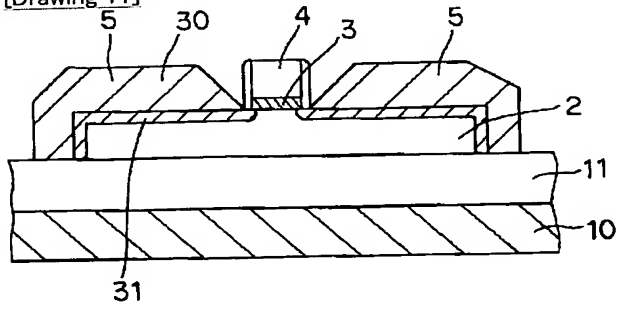
[Drawing 9]



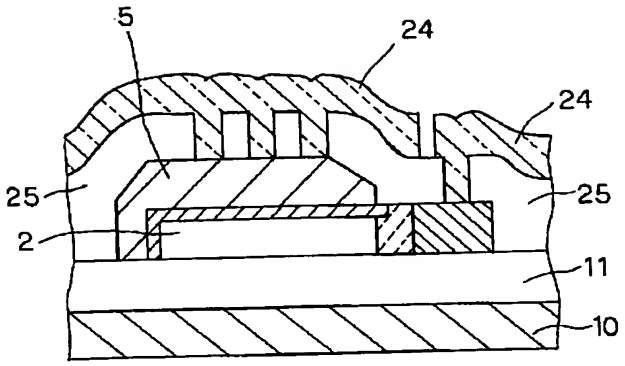
[Drawing 10]



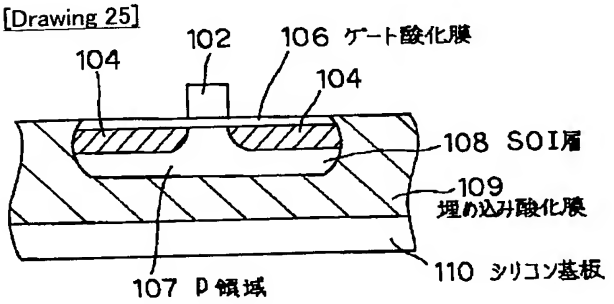
[Drawing 11]



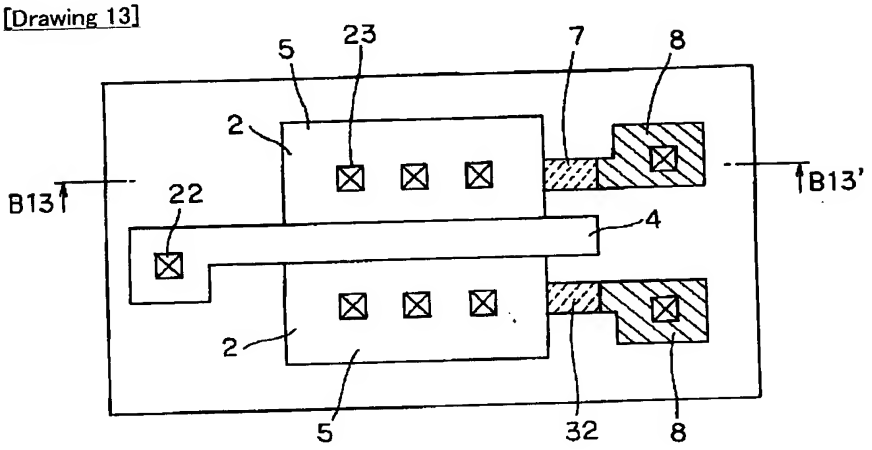
[Drawing 12]



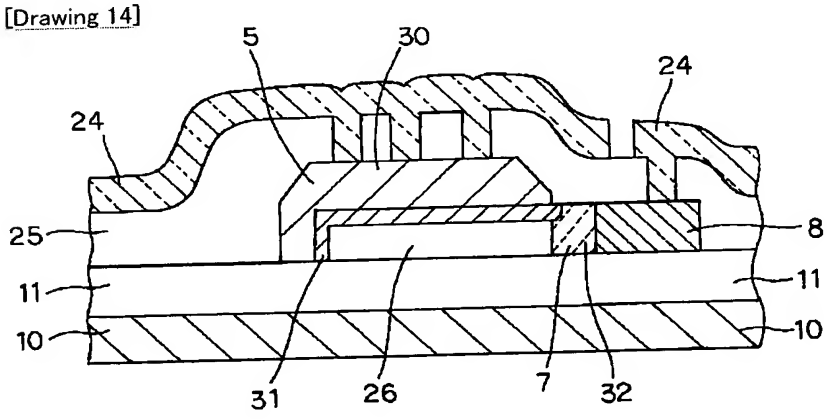
[Drawing 25]



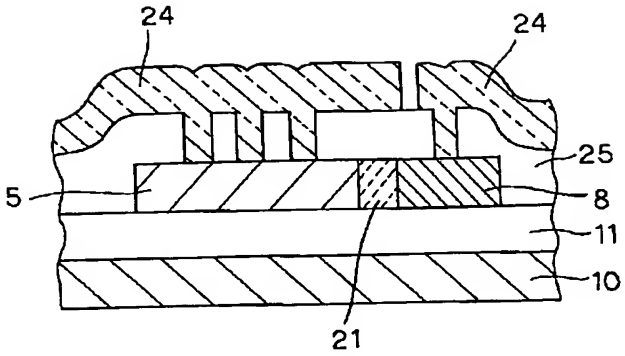
[Drawing 13]



[Drawing 14]



[Drawing 15]



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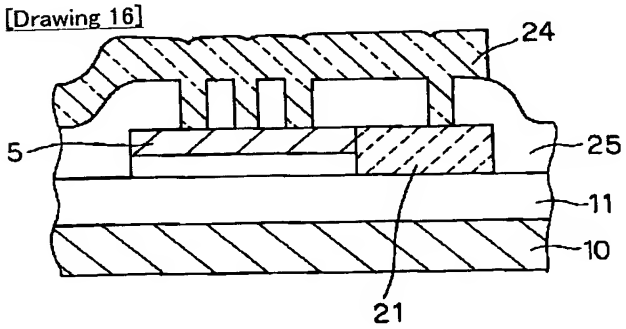

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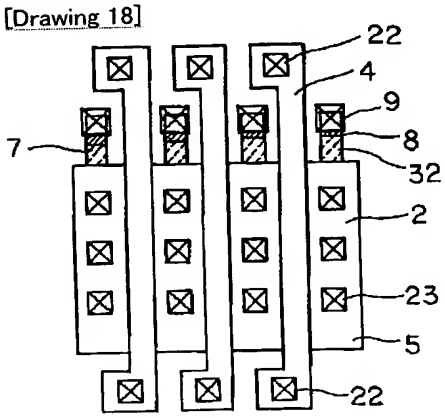

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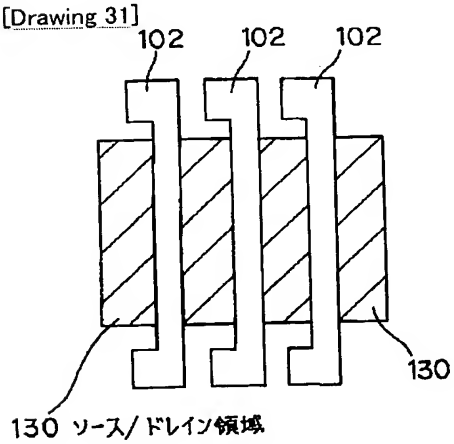

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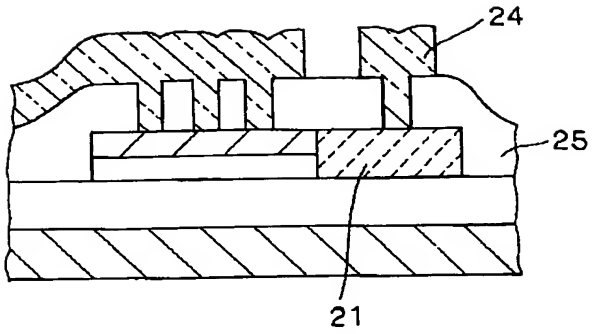

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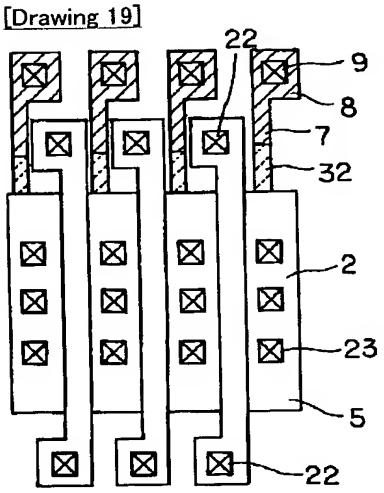

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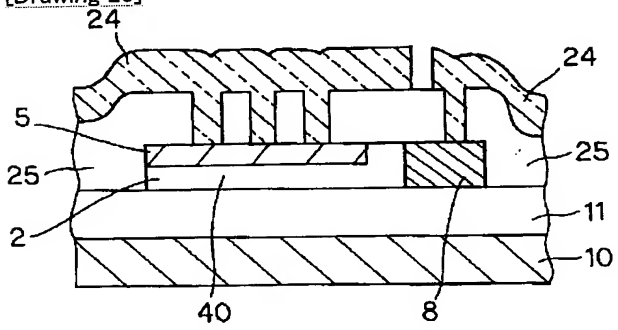

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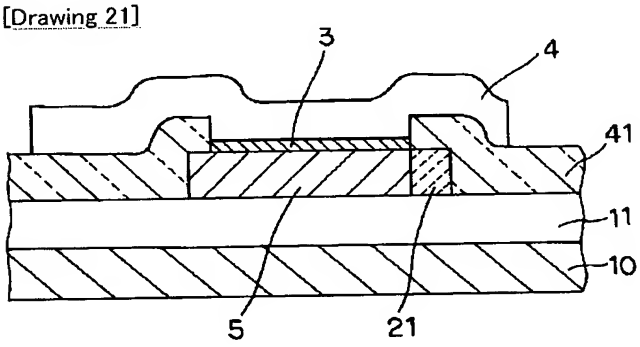

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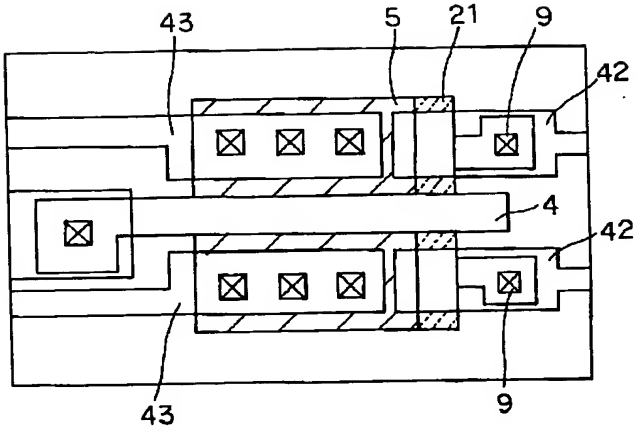

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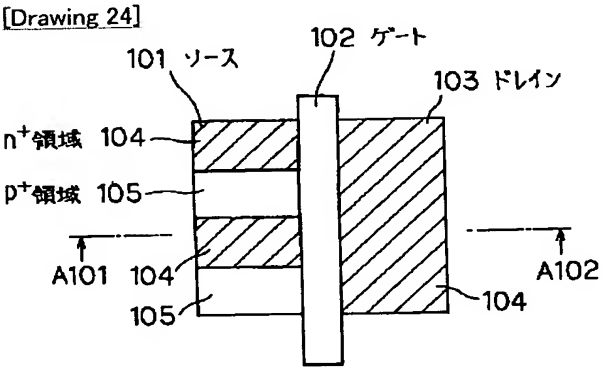

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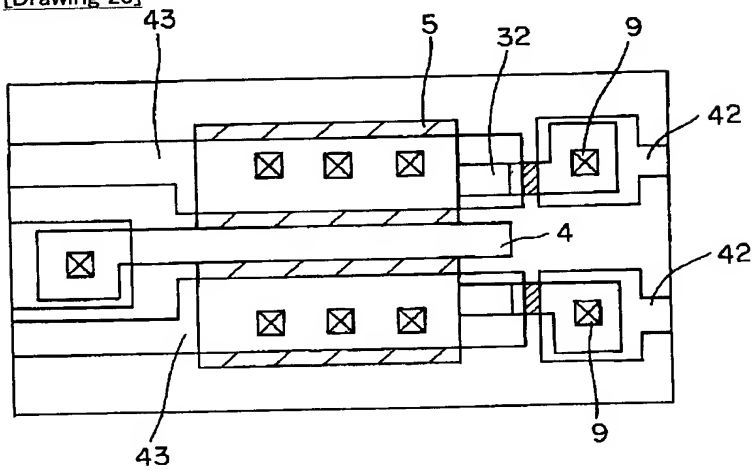

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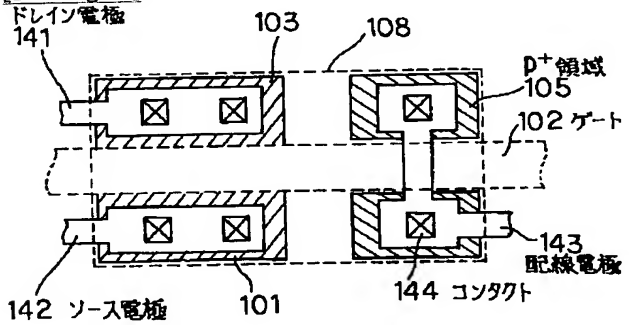

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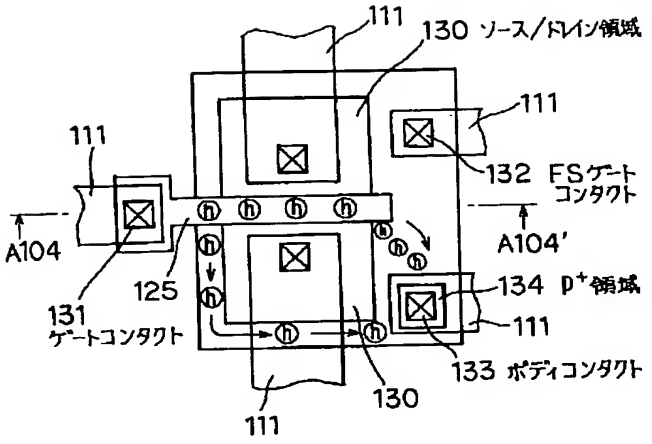

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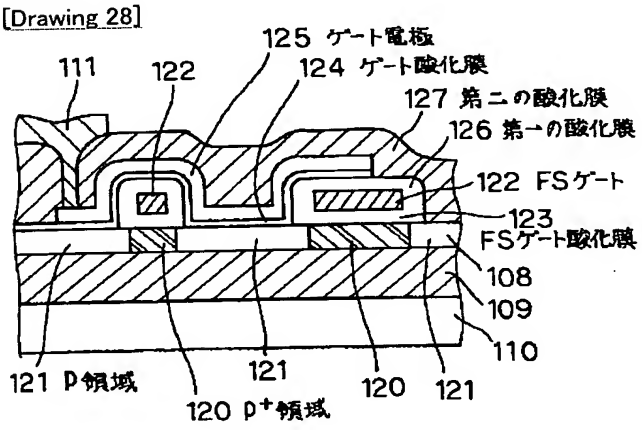

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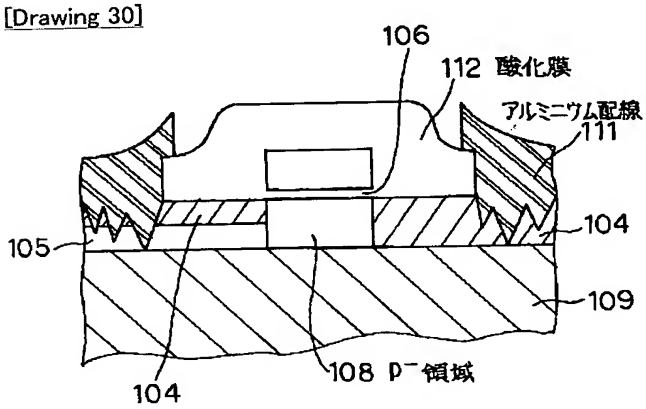

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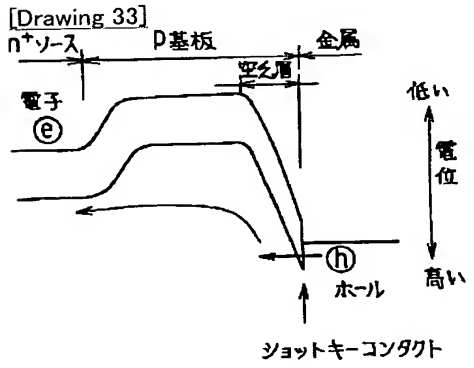

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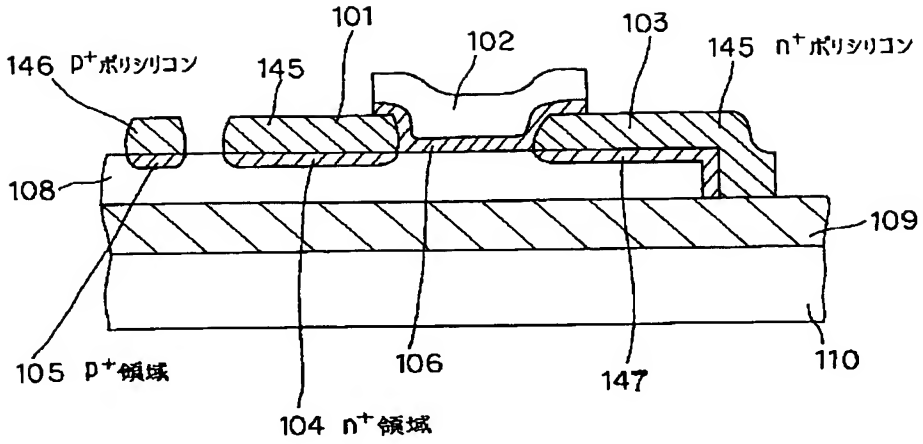

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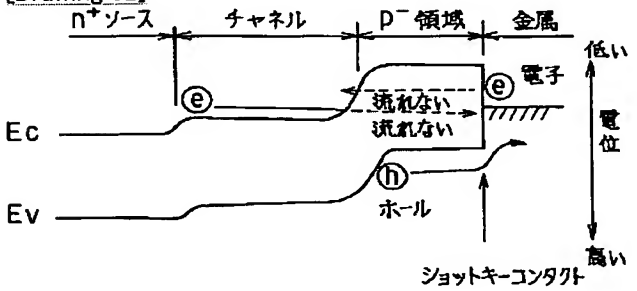
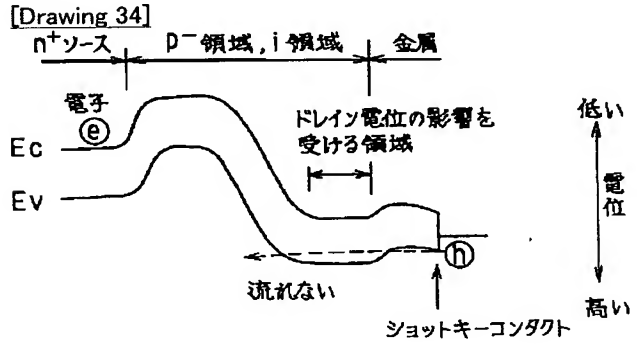


[Drawing 34]



[Translation done.]